CPLD Development/Programmer Kit

User Guide

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Section 1
Introduction

1.1 CPLD Development/ Programmer Kit

The Atmel CPLD Development/Programmer Kit (P/N: ATF15xx-DK2) is a complete development system and an In-System Programming (ISP) programmer for the ATF15xx family of industry-standard pin-compatible Complex Programmable Logic Devices (CPLDs) with Logic Doubling™ features. This kit provides designers a very quick and easy way to develop, prototype and evaluate new designs with an ATF15xx CPLD. With the availability of the different Socket Adapter Boards to support all the package types offered in the ATF15xx family of ISP CPLDs, this CPLD Development/Programmer Board can be used as an ISP programmer to program the ATF15xx ISP CPLDs in all the available package types through the industry-standard JTAG interface (IEEE 1149.1a-1993).

Figure 1-1. Contents of the ATF15xx-DK2

1.2 Kit Contents

- CPLD Development/Programmer Board
- 84-lead PLCC Socket Adapter Board (P/N: ATF15xx-SAJ84)(1)
- Atmel CPLD ISP Download Cable
- Atmel PLD Software CD-ROM (includes ProChip Designer™, Atmel-WinCUPL™ and other EPLD software)
- Atmel CD-ROM Data Books
- One ATF1508AS 5V 84-lead PLCC Sample Device
- One ATF1508ASVL 3.3V, low-power, 84-lead PLCC Sample Device
- Atmel CPLD Development/Programmer Kit User Guide

Note: 1. Only the 84-lead PLCC Socket Adapter Board is included in this kit. Other Socket Adapter Boards are sold separately. Please refer to Section 1.6 for ordering information of the Socket Adapter Boards.

1.3 Kit Features

1.3.1 CPLD Development/ Programmer Board

- 10-lead JTAG-ISP Port
- Regulated Power Supply Circuitry for 9V DC Power Source
- 5V or 3.3V V_{CC} Operation
- 84-lead PLCC Socket Adapter Board
- Socket Adapter Board Headers
- Expansion Terminal Holes for all Input and I/O pins of the ATF15xx Device
- 2 MHz Crystal Oscillator
- Eight 8-segment LED Displays
- Global Clear and Output Enable Push Button Switches

1.3.2 Logic Doubling CPLDs

- ATF1508AS-15JC84, 5V 128-Macrocell ISP CPLD with Logic Doubling Architecture
- ATF1508ASVL-20JC84, 3.3V Low-power 128-Macrocell ISP CPLD with Logic Doubling Architecture

1.3.3 CPLD ISP Download Cable

- 5V/3.3V ISP Download Cable for PC Parallel Printer (LPT) Port

1.3.4 PLD Software CD-ROM

- Free Atmel-WinCUPL™ Design Software
- 30-day Trial Version of Atmel ProChip Designer™ Software
- Full Licensed Version of Atmel ProChip Designer Software (permanent license required)
- Atmel CPLD ISP Software (ATMISP)
- POF2JED Conversion Utility
- Logic Doubling Support and Documentation

1.3.5 Atmel CD-ROM Data Books

- Data Sheets
- Application Notes
- Manuals and User Guides

1.4 Device Support

The Atmel CPLD Development/Programmer Board supports the following devices in all speed grades and packages:

ATF1502AS/ASL	ATF1508AS/ASL
ATF1502ASV	ATF1508ASV/ASVL
ATF1502SE/SEL	ATF1508SE/SEL
ATF1502AE/AEL	ATF1508AE/AEL
ATF1504AS/ASL	ATF1516SE/SEL (Future)
ATF1504ASV/ASVL	ATF1516AE/AEL (Future)
ATF1504SE/SEL	ATF1532AE/AEL (Future)
ATF1504AE/AEL	

1.5 System Requirements

The minimum hardware and software requirements to program an ATF15xx ISP CPLD on the CPLD Development/Programmer Board through the Atmel CPLD ISP Software (ATMISP) V4.0 or later are:

- Pentium® or Pentium-compatible microprocessor based computer
- Windows® 98, Windows NT® 4.0, Windows ME, or Windows 2000
- 16-MByte RAM
- 10-MByte free hard disk space
- Windows-supported mouse
- Available parallel printer (LPT) port
- 9V DC power supply with 500 mA of supply current
- SVGA monitor (800 x 600 resolution)

1.6 Ordering Information

Part Number	Description
ATF15xx-DK2	Atmel CPLD Development/Programmer Kit
ATF15xx-SAA44	44-lead TQFP Socket Adapter Board
ATF15xx-SAJ44	44-lead PLCC Socket Adapter Board
ATF15xx-SAC49	49-lead BGA Socket Adapter Board
ATF15xx-SAJ68	68-lead PLCC Socket Adapter Board
ATF15xx-SAJ84	84-lead PLCC Socket Adapter Board
ATF15xx-SAA100	100-lead TQFP Socket Adapter Board
ATF15xx-SAQ100	100-lead PQFP Socket Adapter Board
ATF15xx-SACT100	100-lead BGA Socket Adapter Board
ATF15xx-SAA144	144-lead TQFP Socket Adapter Board
ATF15xx-SAQ160	160-lead PQFP Socket Adapter Board
ATF15xx-SAC169	169-lead BGA Socket Adapter Board
ATF15xx-SAQ208	208-lead PQFP Socket Adapter Board
ATF15xx-SACT256	256-lead BGA Socket Adapter Board

1.7 Technical Support

For technical support on any Atmel PLD related issues, please contact the Atmel PLD Applications Group at:

Hotline: 1-408-436-4333

Email: pld@atmel.com

URL: www.atmel.com/atmel

1.8 References

To help PLD designers use the different Atmel PLD software, documentation such as Help Files, Tutorials, Application Notes/Briefs, and User Guides are available.

1.8.1 ProChip Designer

ProChip Designer Help Files	From the ProChip Designer main window, click on HELP and then select PROCHIP DESIGNER HELP.
Tutorials	From the ProChip Designer main window, click on HELP and then select TUTORIALS.
Known Problems & Solutions	From the ProChip Designer main window, click on HELP and then select REVIEW KPS.

1.8.2 Atmel-WinCUPL

Help Files	From the Atmel-WinCUPL main window, click on HELP and then select CONTENTS.
CUPL Programmers Reference Guide	From the Atmel-WinCUPL main window, click on HELP and then select CUPL PROGRAMMERS REFERENCE.
Tutorial	From the Atmel-WinCUPL main window, click on HELP, select ATMEL INFO and then select TUTORIAL1.PDF.
Known Problems & Solutions	From the Atmel-WinCUPL main window, click on HELP, select ATMEL INFO and then select CUPL_BUG.PDF.

1.8.3 ATMISP

Help Files	From the ATMISP main window, click on HELP and then select ISP HELP.
Tutorial	From the ATMISP main window, click on HELP, and then select ATMISP TUTORIAL.
Known Problems & Solutions	Using Windows Explorer, go to the directory where ATMISP is installed and open the README.TXT file through any ASCII text editor.

1.8.4 POF2JED

ATF15xx Conversion Application Brief	From the POF2JED main window, click on HELP and then select CONVERSION OPTIONS.

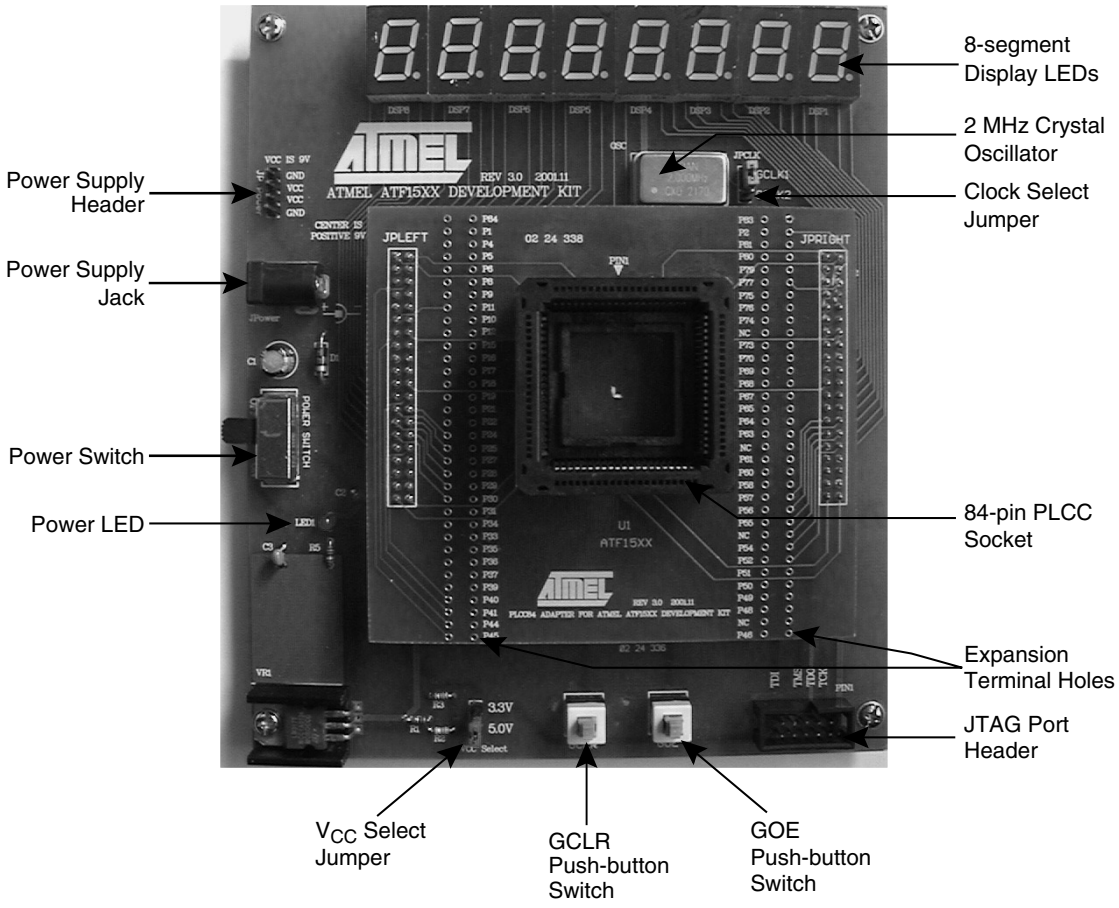
Section 2

Hardware Description

2.1 Atmel CPLD Development/ Programmer Board

The Atmel CPLD Development/Programmer Board, along with the Socket Adapter Board as shown in Figure 2-1, contains many features that designers will find very useful when developing, prototyping, or evaluating their ATF15xx CPLD design. Features such as push-button switches, 8-segment display LEDs, 2 MHz crystal oscillator, 5V/3.3V V_{CC} selector, JTAG-ISP port, and expansion terminal holes make this a very versatile starter/development kit and an ISP programmer for the ATF15xx family of JTAG-ISP CPLDs.

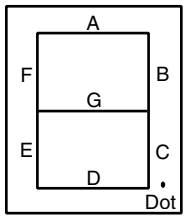
Figure 2-1. CPLD Development/Programmer Board with 84-lead PLCC Socket Adapter Board



2.1.1 8-segment Display LEDs

The Atmel CPLD Development/Programmer Board contains eight 8-segment LEDs to allow the designer to observe the outputs of the ATF15xx. These eight LEDs are labeled **DSP1** to **DSP8** on the board. These eight display LEDs are common anode LEDs with the common anode lines connected to V_{CC} and the individual cathode lines connected to the I/O pins of the ATF15xx CPLD on the CPLD Development/Programmer Board. To turn on a particular segment of an LED, the corresponding ATF15xx I/O pin connected to this LED segment must be in a logical-0 state. Hence, the outputs of the ATF15xx need to be configured as active-low outputs in the design file.

Figure 2-2. 8-segment Display LED



Each segment of the display LED is hard-wired to one specific I/O pin of the ATF15xx. For the higher pin count devices (100-lead and larger), all eight segments of the eight LEDs are connected to the I/O pins of the ATF15xx. However, for the lower pin count devices (84-lead and smaller), only a subset of the LED segments are connected to the ATF15xx's I/O pins. Table 2-1 to Table 2-8 below show the connections of the LEDs to the ATF15xx in all the different package types.

Table 2-1. Connections of LEDs to ATF15xx 44-lead PLCC

DSP/Sgt	PLD Pin #
1/A	NC
1/B	NC
1/C	NC
1/D	NC
1/E	NC
1/F	NC
1/G	NC
1/DOT	NC
2/A	NC
2/B	NC
2/C	NC
2/D	NC
2/E	NC
2/F	NC
2/G	NC
2/DOT	NC

DSP/Sgt	PLD Pin #
3/A	28
3/B	26
3/C	24
3/D	25
3/E	27
3/F	29
3/G	31
3/DOT	NC
4/A	36
4/B	33
4/C	34
4/D	40
4/E	37
4/F	39
4/G	41
4/DOT	NC

DSP/Sgt	PLD Pin #
5/A	6
5/B	4
5/C	5
5/D	8
5/E	11
5/F	9
5/G	12
5/DOT	NC
6/A	18
6/B	16
6/C	14
6/D	17
6/E	19
6/F	20
6/G	21
6/DOT	NC

DSP/Sgt	PLD Pin #
7/A	NC
7/B	NC
7/C	NC
7/D	NC
7/E	NC
7/F	NC
7/G	NC
7/DOT	NC
8/A	NC
8/B	NC
8/C	NC
8/D	NC
8/E	NC
8/F	NC
8/G	NC
8/DOT	NC

Table 2-2. Connections of LEDs to ATF15xx 44-lead TQFP

DSP/Sgt	PLD Pin #
1/A	NC
1/B	NC
1/C	NC
1/D	NC
1/E	NC
1/F	NC
1/G	NC
1/DOT	NC
2/A	NC
2/B	NC
2/C	NC
2/D	NC
2/E	NC
2/F	NC
2/G	NC
2/DOT	NC

DSP/Sgt	PLD Pin #
3/A	21
3/B	19
3/C	18
3/D	20
3/E	22
3/F	23
3/G	25
3/DOT	NC
4/A	30
4/B	27
4/C	28
4/D	34
4/E	31
4/F	33
4/G	35
4/DOT	NC

DSP/Sgt	PLD Pin #
5/A	44
5/B	42
5/C	43
5/D	2
5/E	5
5/F	3
5/G	6
5/DOT	NC
6/A	12
6/B	10
6/C	8
6/D	11
6/E	13
6/F	14
6/G	15
6/DOT	NC

DSP/Sgt	PLD Pin #
7/A	NC
7/B	NC
7/C	NC
7/D	NC
7/E	NC
7/F	NC
7/G	NC
7/DOT	NC
8/A	NC
8/B	NC
8/C	NC
8/D	NC
8/E	NC
8/F	NC
8/G	NC
8/DOT	NC

Table 2-3. Connections of LEDs to ATF15xx 68-lead PLCC

DSP/Sgt	PLD Pin #
1/A	NC
1/B	NC
1/C	NC
1/D	NC
1/E	NC
1/F	NC
1/G	NC
1/DOT	NC
2/A	37
2/B	33
2/C	36
2/D	39
2/E	41
2/F	40
2/G	42
2/DOT	NC

DSP/Sgt	PLD Pin #
3/A	47
3/B	45
3/C	44
3/D	46
3/E	49
3/F	51
3/G	52
3/DOT	NC
4/A	56
4/B	54
4/C	55
4/D	61
4/E	59
4/F	60
4/G	64
4/DOT	NC

DSP/Sgt	PLD Pin #
5/A	5
5/B	4
5/C	7
5/D	9
5/E	13
5/F	8
5/G	10
5/DOT	NC
6/A	17
6/B	14
6/C	15
6/D	18
6/E	22
6/F	20
6/G	23
6/DOT	NC

DSP/Sgt	PLD Pin #
7/A	25
7/B	24
7/C	27
7/D	29
7/E	32
7/F	28
7/G	30
7/DOT	NC
8/A	NC
8/B	NC
8/C	NC
8/D	NC
8/E	NC
8/F	NC
8/G	NC
8/DOT	NC

Table 2-4. Connections of LEDs to ATF15xx 84-lead PLCC

DSP/Sgt	PLD Pin #
1/A	49
1/B	46
1/C	48
1/D	50
1/E	52
1/F	51
1/G	54
1/DOT	NC
2/A	57
2/B	55
2/C	56
2/D	58
2/E	61
2/F	60
2/G	63
2/DOT	NC

DSP/Sgt	PLD Pin #
3/A	67
3/B	64
3/C	65
3/D	68
3/E	70
3/F	69
3/G	73
3/DOT	NC
4/A	76
4/B	74
4/C	75
4/D	77
4/E	80
4/F	79
4/G	81
4/DOT	NC

DSP/Sgt	PLD Pin #
5/A	6
5/B	4
5/C	5
5/D	8
5/E	10
5/F	9
5/G	11
5/DOT	45
6/A	16
6/B	12
6/C	15
6/D	17
6/E	20
6/F	18
6/G	21
6/DOT	44

DSP/Sgt	PLD Pin #
7/A	25
7/B	22
7/C	24
7/D	27
7/E	29
7/F	28
7/G	30
7/DOT	41
8/A	34
8/B	31
8/C	33
8/D	35
8/E	37
8/F	36
8/G	39
8/DOT	40

Table 2-5. Connections of LEDs to ATF15xx 100-lead TQFP

DSP/Sgt	PLD Pin #
1/A	47
1/B	52
1/C	48
1/D	46
1/E	44
1/F	45
1/G	42
1/DOT	49
2/A	54
2/B	41
2/C	40
2/D	56
2/E	58
2/F	57
2/G	60
2/DOT	55

DSP/Sgt	PLD Pin #
3/A	67
3/B	64
3/C	63
3/D	65
3/E	68
3/F	69
3/G	71
3/DOT	61
4/A	80
4/B	76
4/C	78
4/D	84
4/E	81
4/F	83
4/G	85
4/DOT	75

DSP/Sgt	PLD Pin #
5/A	96
5/B	93
5/C	94
5/D	97
5/E	99
5/F	98
5/G	100
5/DOT	92
6/A	12
6/B	9
6/C	8
6/D	10
6/E	13
6/F	14
6/G	16
6/DOT	6

DSP/Sgt	PLD Pin #
7/A	20
7/B	17
7/C	19
7/D	21
7/E	25
7/F	23
7/G	29
7/DOT	22
8/A	32
8/B	30
8/C	31
8/D	33
8/E	36
8/F	35
8/G	37
8/DOT	28

Table 2-6. Connections of LEDs to ATF15xx 100-lead PQFP

DSP/Sgt	PLD Pin #
1/A	48
1/B	50
1/C	49
1/D	47
1/E	44
1/F	46
1/G	43
1/DOT	51
2/A	56
2/B	54
2/C	42
2/D	58
2/E	60
2/F	59
2/G	62
2/DOT	52

DSP/Sgt	PLD Pin #
3/A	69
3/B	66
3/C	65
3/D	67
3/E	70
3/F	71
3/G	73
3/DOT	63
4/A	82
4/B	78
4/C	81
4/D	86
4/E	83
4/F	85
4/G	87
4/DOT	77

DSP/Sgt	PLD Pin #
5/A	98
5/B	95
5/C	96
5/D	99
5/E	3
5/F	100
5/G	4
5/DOT	94
6/A	14
6/B	11
6/C	10
6/D	12
6/E	15
6/F	16
6/G	18
6/DOT	8

DSP/Sgt	PLD Pin #
7/A	22
7/B	19
7/C	21
7/D	23
7/E	27
7/F	25
7/G	39
7/DOT	24
8/A	37
8/B	38
8/C	35
8/D	33
8/E	31
8/F	34
8/G	32
8/DOT	30

Table 2-7. Connections of LEDs to ATF15xx 144-lead TQFP

DSP/Sgt	PLD Pin #
1/A	79
1/B	78
1/C	74
1/D	80
1/E	82
1/F	81
1/G	83
1/DOT	77
2/A	88
2/B	86
2/C	87
2/D	91
2/E	93
2/F	92
2/G	94
2/DOT	84

DSP/Sgt	PLD Pin #
3/A	100
3/B	98
3/C	99
3/D	101
3/E	106
3/F	102
3/G	107
3/DOT	97
4/A	118
4/B	119
4/C	117
4/D	114
4/E	112
4/F	116
4/G	113
4/DOT	111

DSP/Sgt	PLD Pin #
5/A	134
5/B	137
5/C	136
5/D	133
5/E	138
5/F	132
5/G	131
5/DOT	139
6/A	9
6/B	7
6/C	6
6/D	8
6/E	10
6/F	11
6/G	15
6/DOT	5

DSP/Sgt	PLD Pin #
7/A	25
7/B	22
7/C	23
7/D	26
7/E	28
7/F	27
7/G	29
7/DOT	21
8/A	41
8/B	31
8/C	32
8/D	38
8/E	37
8/F	40
8/G	39
8/DOT	30

Table 2-8. Connections of LEDs to ATF15xx 160-lead PQFP

DSP/Sgt	PLD Pin #	DSP/Sgt	PLD Pin #	DSP/Sgt	PLD Pin #	DSP/Sgt	PLD Pin #
1/A	91	3/A	102	5/A	11	7/A	29
1/B	89	3/B	100	5/B	159	7/B	27
1/C	90	3/C	98	5/C	160	7/C	28
1/D	80	3/D	101	5/D	10	7/D	52
1/E	73	3/E	103	5/E	12	7/E	50
1/F	78	3/F	105	5/F	13	7/F	53
1/G	72	3/G	106	5/G	14	7/G	51
1/DOT	88	3/DOT	97	5/DOT	158	7/DOT	25
2/A	69	4/A	110	6/A	20	8/A	43
2/B	71	4/B	108	6/B	18	8/B	49
2/C	68	4/C	109	6/C	16	8/C	30
2/D	92	4/D	123	6/D	19	8/D	31
2/E	94	4/E	111	6/E	21	8/E	32
2/F	93	4/F	121	6/F	23	8/F	41
2/G	96	4/G	122	6/G	24	8/G	33
2/DOT	70	4/DOT	107	6/DOT	15	8/DOT	48

2.1.2 Push-button Switches

Two push-button switches are provided to allow the user to control the logic states of the OE1 and GCLR inputs of the ATF15xx. These two switches are labeled GOE and GCLR on the board. The GCLR push-button switch is a momentary Single-Pole Single-Throw (SPST) normally open switch while the GOE push-button switch is a snap-acting momentary SPST normally open switch. As shown in the CPLD Development/Programmer Board schematic in Figure 4-1, these two switches are normally open and the GCLR and GOE signals are pulled-up to V_{CC} when they are not depressed. When the switches are depressed, the GCLR and GOE signals are connected to GND.

The output of the GCLR switch is connected to the GCLR dedicated input pin of the ATF15xx, and it is intended to be used as an active-low reset signal to reset the registers in the ATF15xx. The output of the GOE switch is connected to the OE1 dedicated input pin of the ATF15xx. It is intended to be used as an active-high or active-low output enable signal to control the enabling/disabling of the tri-state output buffers in the ATF15xx. However, these two switches can also be used to generate general logic input signals to the GCLR and OE1 input pins of the ATF15xx.

2.1.3 Clock Select Jumper

The Clock Select Jumper, labeled JPCLK, on the CPLD Development/Programmer Board is a two-position jumper that allows the user to select which GCLK dedicated input pin (either GCLK1 or GCLK2) of the ATF15xx should be connected to the output of the 2 MHz crystal oscillator. In addition, the jumper can be removed to allow an external clock source to be connected to GCLK1 and/or GCLK2 of the ATF15xx.

Table 2-9 shows the pin numbers for the GCLR, OE1, GCLK1 and GCLK2 dedicated input pins of the ATF15xx in all the available package types.

Table 2-9. Pin Numbers of GCLR, OE1, GCLK1 and GCLK2

Signal	44-lead TQFP	44-lead PLCC	68-lead PLCC	84-lead PLCC	100-lead PQFP	100-lead TQFP	144-lead TQFP	160-lead PQFP
GCLR	39	1	1	1	91	89	127	141
OE1	38	44	68	84	90	88	126	140
GCLK1	37	43	67	83	89	87	125	139
GCLK2	40	2	2	2	92	90	128	142

2.1.4 V_{CC} Select Jumper

The V_{CC} Select Jumper, labeled VCC Select, on the CPLD Development/Programmer Board is a two-position jumper that allows the users to select the V_{CC} voltage level (either 3.3V or 5.0V) used by various components on the CPLD Development/Programmer Board. This voltage generated by the on-board voltage regulation circuitry is applied to the V_{CC} input pins (both VccINT and VccIO) of the ATF15xx, the common anode lines of the eight 8-segment LEDs, the V_{CC} input of the 2 MHz crystal oscillator, the two push-button switches, and the V_{CC} pin (Pin 4) of the 10-pin JTAG port header labeled JTAG.

Therefore, when a 3.3V device (ATF15xxASV/ASVL/AE/AEL) is used on this board, the V_{CC} Select Jumper must be in the 3.3V position. On the other hand, when a 5V device (ATF15xxAS/ASL/SE/SEL) is used on this board, the V_{CC} Select Jumper must be in the 5.0V position. This is also true when the ATF15xx is being programmed through ISP on this board.

2.1.5 JTAG Port Header

The JTAG Port Header, labeled JTAG, on the CPLD Development/Programmer Board is used to connect the ATF15xx's JTAG port pins (TCK, TDI, TMS and TDO) through the ISP download cable to the parallel printer (LPT) port of a PC for ISP programming of the ATF15xx. Table 2-10 shows the pin numbers for the four JTAG port pins of the ATF15xx in all the available package types.

Table 2-10. Pin Numbers of JTAG Port Signals

Signal	44-lead TQFP	44-lead PLCC	68-lead PLCC	84-lead PLCC	100-lead PQFP	100-lead TQFP	144-lead TQFP	160-lead PQFP
TDI	1	7	12	14	6	4	4	9
TDO	32	38	57	71	75	73	104	112
TMS	7	13	19	23	17	15	20	22
TCK	26	32	50	62	64	62	89	99

The ISP algorithm is controlled by the ATMISP software, which runs on the PC. The four JTAG signals are generated by the LPT port and they are buffered by the ISP download cable before going into the ATF15xx on the CPLD Development/Programmer Board. The pinout for the 10-pin JTAG Port Header on the CPLD Development/Programmer Board is shown in Figure 2-3 and the dimensions of this 10-pin male JTAG header are shown in Figure 2-4.

Figure 2-3. Pinout Diagram of 10-pin JTAG Port Header (Top-view)

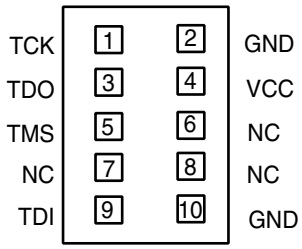
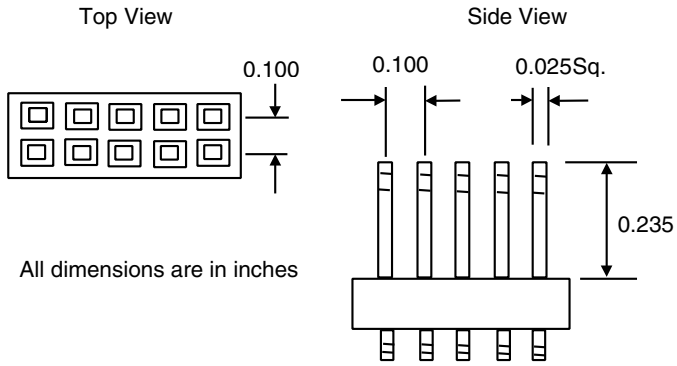


Figure 2-4. 10-pin Male Header Dimensions



The pinout of this 10-pin JTAG Port Header is compatible with the Altera® ByteBlaster™ and ByteBlasterMV™ cables. In addition, the ATMISP software allows users to choose either the Atmel CPLD ISP Cable or the ByteBlaster/ByteBlasterMV cable to implement ISP.

2.1.6 Power Connectors

The Atmel CPLD Development/Programmer Board contains two different types of power connectors, and either one can be used to connect to a 9V DC power source to power the board. The first power connector, labeled JPower, is a barrel power jack with a 2.1 mm diameter post and it mates to a 2.1 mm (inner diameter) x 5.5 mm (outer diameter) female plug. The second power connector, labeled JP Power, is a 4-pin male 0.1" header with 0.025" square posts. The availability of these two types of power connectors allows the users to choose the type of power supply equipment to use for the CPLD Development/Programmer Board.

2.2 Socket Adapter Board

Atmel CPLD Development/Programmer Socket Adapter Boards are circuit boards that interface with the Atmel CPLD Development/Programmer Board. They are used in conjunction with the CPLD Development/Programmer Board to evaluate/program Atmel ISP CPLDs in different package types. Currently, there are nine Socket Adapter Boards available covering all the package types offered in the ATF15xx family of CPLDs. They include 44-lead PLCC, 44-lead TQFP, 68-lead PLCC, 84-lead PLCC, 100-lead TQFP, 100-lead PQFP, 144-lead TQFP and 160-lead PQFP. New Socket Adapter Boards will become available when new packages are offered.

Each socket adapter board contains a socket for the Atmel ATF15xx device on the top side and male headers on the bottom side. The headers on the bottom side mate with the female headers, labeled **JPLEFT** and **JPRIGHT**, on the CPLD Development/Programmer Board. The eight 8-segment LEDs, push-button switches, JTAG port signals, crystal oscillator, V_{CC}, and GND on the CPLD Development/Programmer Board are connected to the ATF15xx device on the Socket Adapter Board through these two rows of connectors.

2.2.1 Expansion Terminal Holes

Rows of expansion terminal holes suitable for 0.1" headers with 0.025" square posts are available on each of the Socket Adapter Boards to allow users to interface the ATF15xx to an external circuit board. All input and I/O pins except the four JTAG port pins of the ATF15xx are routed to these expansion terminal holes, and the corresponding pin numbers are marked next to the terminal holes. Please refer to the Socket Adapter Board schematics in Section 4 for the pinouts of the expansion terminal holes.

On the bottom side of the Socket Adapter Boards, traces connecting the pairs of expansion terminal holes can be cut to isolate the LEDs, push-button switches and crystal oscillator from the ATF15xx on the Socket Adapter Board. This allows the users to gain complete control and access to all input and I/O pins of the ATF15xx.

2.3 Atmel CPLD ISP Cable

The Atmel CPLD ISP Cable connects the parallel printer (LPT) port of the user's PC to the 10-pin JTAG header on the Atmel CPLD Development/Programmer Board or a custom circuit board. This is shown in Figure 2-5. This ISP cable acts as a buffer to buffer the JTAG signals between the PC's LPT port and the ATF15xx on the circuit board. The circuit schematic of the Atmel CPLD ISP Cable is shown in Figure 4-10 and Figure 4-11. The Power-On LED on the back of the 25-pin male connector housing indicates that the cable is connected properly. Make sure this LED is turned on before using the Atmel CPLD ISP Software (ATMISP).

This ISP cable consists of a 25-pin (DB25) male connector, which is connected to the LPT port of a PC. The 10-pin female plug connects to the 10-pin male JTAG header on the ISP circuit board. The red color stripe on the ribbon cable indicates the orientation of Pin 1 of the female plug. The 10-pin male JTAG header on the CPLD Development/Programmer Board is polarized to prevent users from inserting the female plug in the wrong orientation.

If the user is attempting to program low voltage (3.3V) devices, the user needs to use Rev. 4 or later of the Atmel CPLD ISP Cable. This and later revisions will support both the 3.3V and 5V ATF15xx ISP CPLDs. Earlier revisions of the cable only supported 5V devices.

When programming 3.3V devices, the V_{CC} supplied to the ISP cable should also be 3.3V. Similarly, the V_{CC} supplied to the ISP cable should be 5.0V when programming 5V devices.

Figure 2-5. Atmel ISP Cable Connection to ISP Hardware Board/Circuit Board

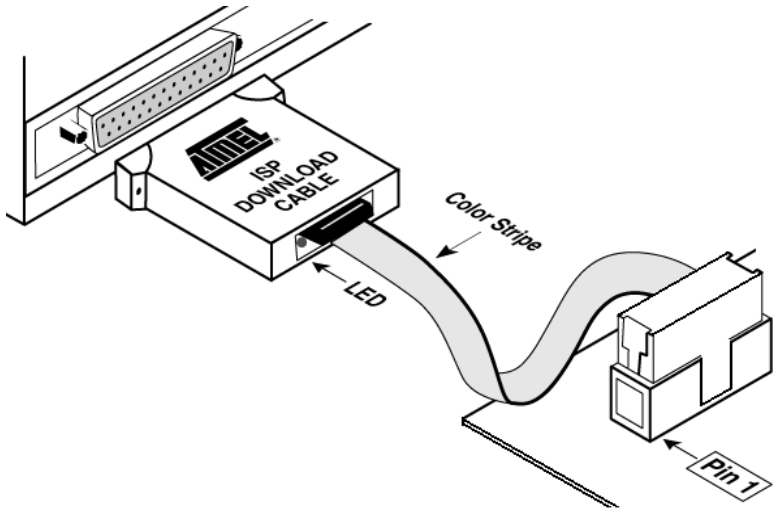
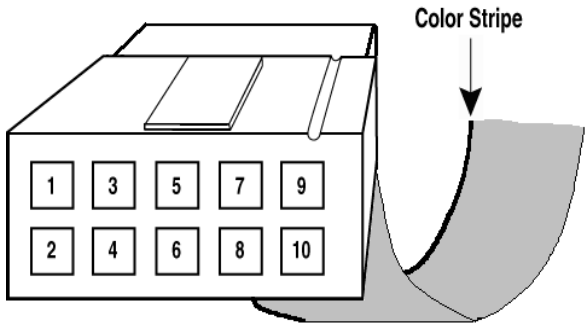


Figure 2-6 shows the pinout for the 10-pin Female header on the Atmel-ISP Cable. The pinout on the 10-pin male header on the PC board (if used for ISP) must match this pinout.

Figure 2-6. Atmel ISP Download Cable 10-pin Female Header Pinout



Note: The user's circuit board must supply VCC and GND to the Atmel CPLD ISP Cable through the 10-pin male header (See Figure 2-3).

Section 3

CPLD Design Flow Tutorial

3.1 Overview

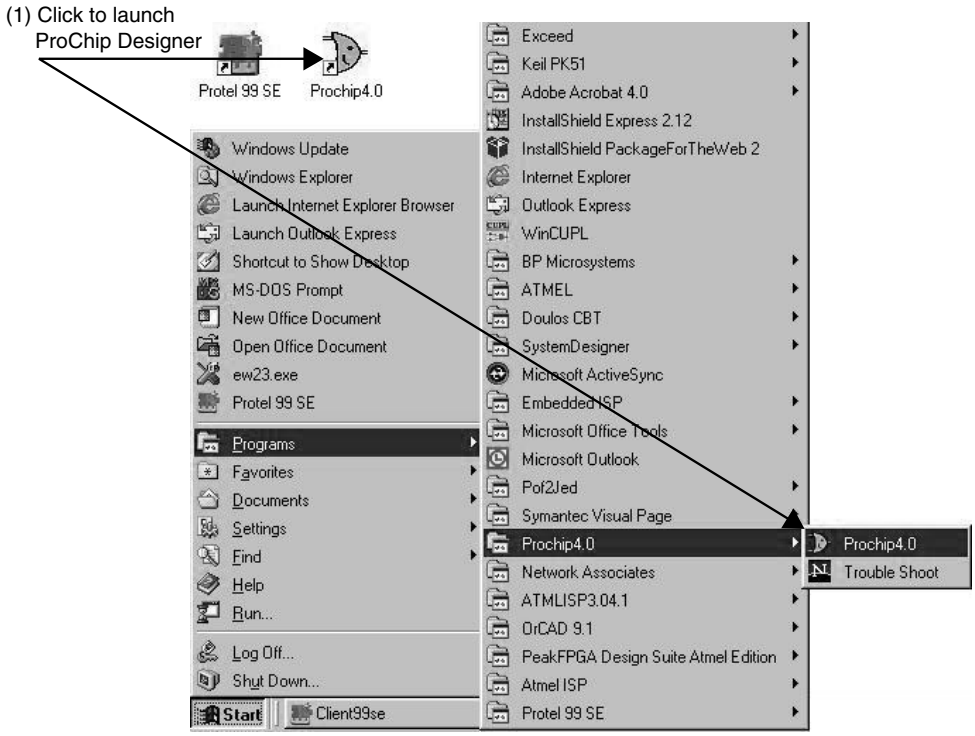
This tutorial will guide the user through a complete design cycle for the Atmel ATF15xx CPLD with Logic Doubling architecture. It will go through each phase of the design cycle step-by-step from design entry, logic synthesis, device fitting, in-system programming, and finally verifying the design on the Atmel CPLD Development/Programming Board.

Note: To complete this tutorial, ProChip Designer V4.0 or later and Atmel-ISP Software (ATMISP) V4.0 or later are required.

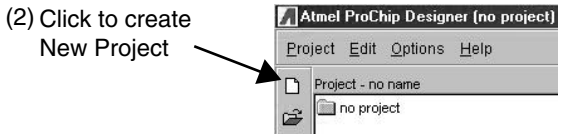
3.2 Create a Project Using the "New Project Wizard"

Before starting the design process, a Project File must be created within ProChip Designer. ProChip Designer's **New Project Wizard** provides a very easy way to create a new Project File.

1. Click on the **START** .... **PROGRAMS** .... **PROCHIP** Icon to launch ProChip Designer. Or double-click on the **PROCHIP** icon on the desktop.



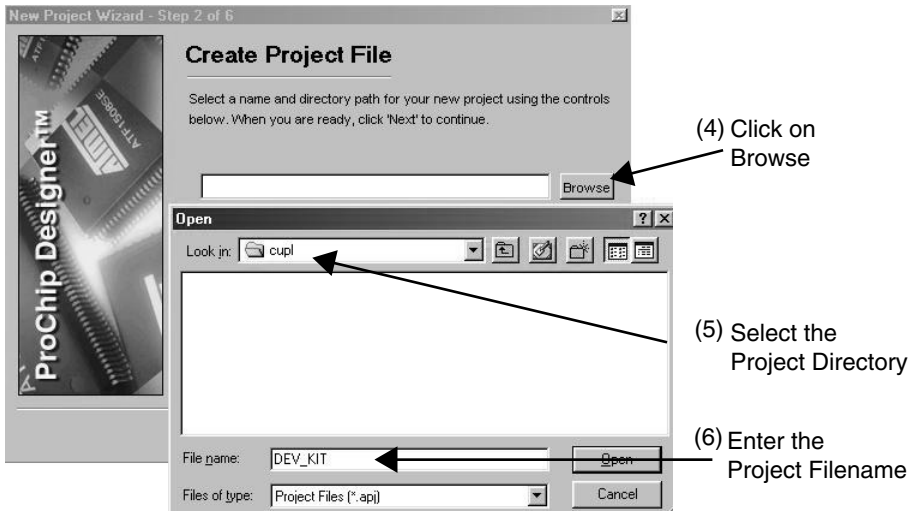
2. Click on **PROJECT** .... **NEW** or double-click on the **NEW PROJECT** shortcut button to launch the New Project Wizard.



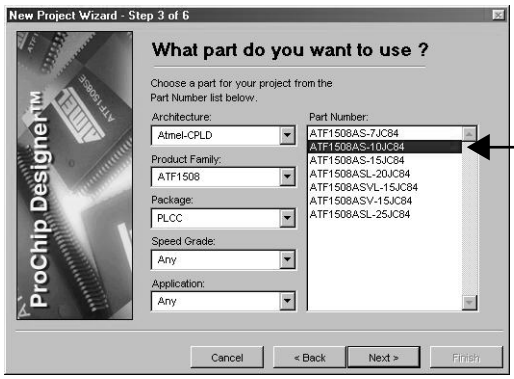
3. Click on the **NEXT** button to start the project file creation process.

4. Click on the **BROWSE** button to open the browser window.
5. Use **C:\PROCHIP\DESIGNS\CUPL** as the directory of the project.
6. Enter **DEV_KIT.APJ** as the project filename. The extension of a project file must be .**APJ**.

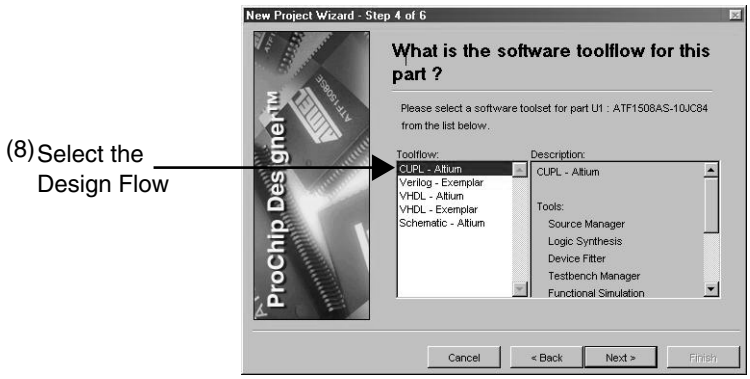
Note: The name and directory of the design project is specified in this window. All design, simulation and other project files must be placed in this project directory.



7. Choose **[ATF1508AS-10JC84]** as the target device type for the project. Also review the *Filters* that allow for selection of a specific *Speed Grade* or *Package Type*.



8. Select **CUPL – ALTIUM** as the software tool for this design flow.



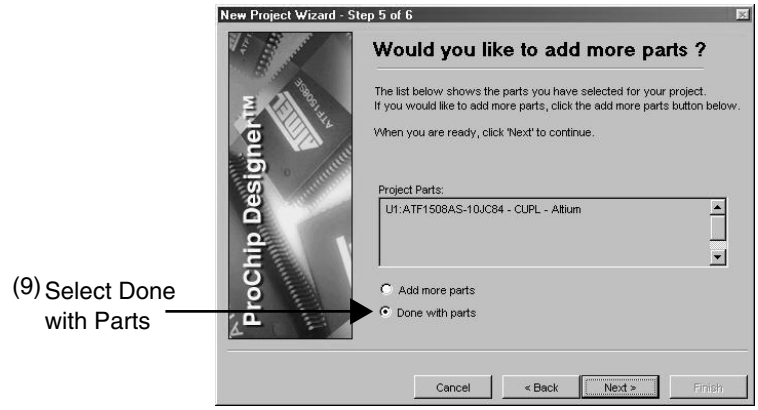
With ProChip Designer V4.0 and later, the five possible design flows and their corresponding design entry types supported are listed in the table below:

Design Flow	Design Entry Type
CUPL – Altium™	CUPL design entry through Altium Protel™ 99SE
Verilog – Exemplar™(1)	Verilog® design entry through Exemplar Leonardo Spectrum™
VHDL – Altium	VHDL design entry through the Altium PeakFPGA
VHDL – Exemplar(1)	VHDL design entry through Exemplar Leonardo Spectrum
Schematic – Altium	Schematic design entry through Altium Protel 99SE

Note: 1. Design flow require Mentor Graphics® Leonardo Spectrum software with Atmel CPLD support.

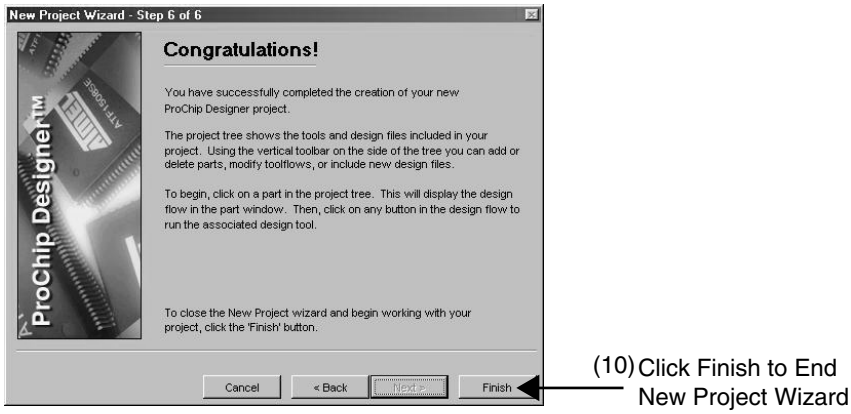
9. Select **DONE WITH PARTS** so that there will be only one device in this project.

On the other hand, users can select **ADD MORE PARTS** to include more parts to the current Project Directory.

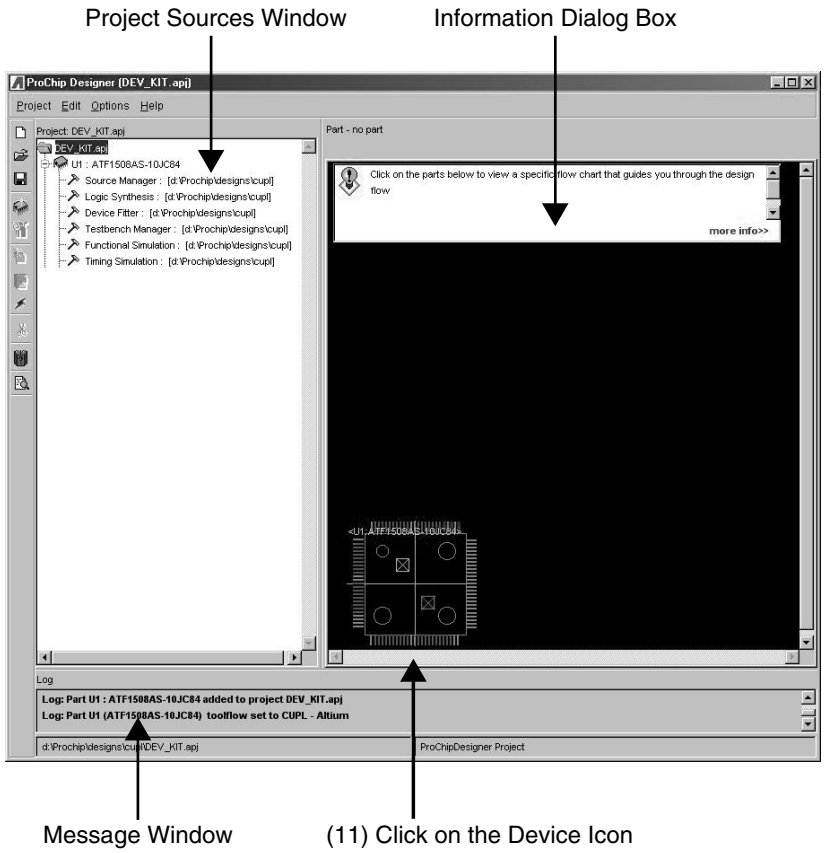


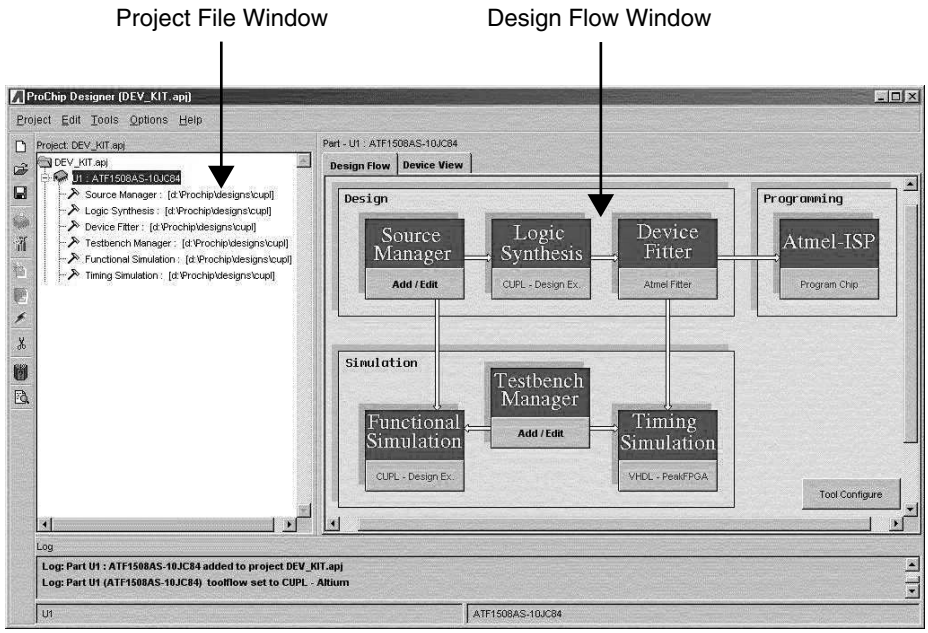
10. Click the **FINISH** button to finish the New Project Wizard and the project creation process.

This closes the *New Project Wizard* and opens the *ProChip Designer* window. The *Sources* in the project are shown in the Left window.



11. Click on the **Device Icon [ATF1508AS-10JC84]** to view the *Design Flow* window.

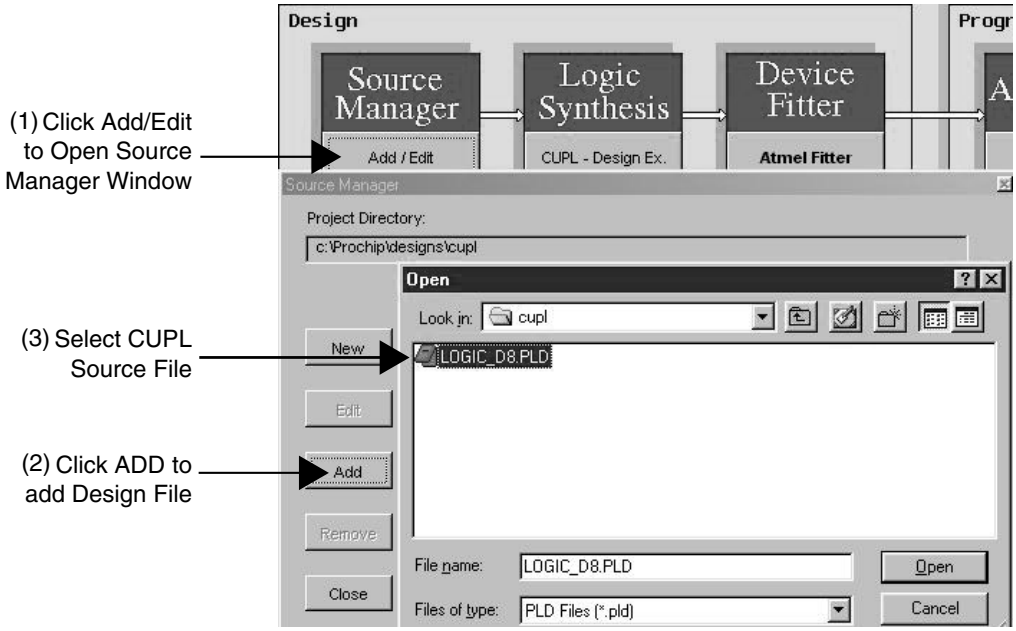




3.3 Add a Design File

Once the Project File is created, the next step is to add the design source file(s) into the user's project. For this tutorial, a single CUPL design file will be added into the project.

1. Click on the **ADD/EDIT** button from *Source Manager* to open the *Source Manager Window*. The user can view the *Source Manager* Help File by clicking on the **Help** button within the *Source Manager Window* to view the description for the different processes.
2. In the *Source Manager Window*, click on the **ADD** button to add a CUPL design file to the project.
3. In the *File Manager Window*, select **LOGIC_D8.PLD** from the *C:\PROCHIP\DESIGNS\CUPL* directory as the source design file for this project.



This "LOGIC_D8.PLD" is a CUPL design that uses the eight 8-segment LED displays and the 2 MHz oscillator on the Atmel CPLD Development/Programmer Board to generate a scrolling message that displays the words "logic doubling" on the LEDs. The GOE push-button switch is used to control the direction that the message scrolls in (left or right). The GCLR push-button switch is used to reset the counter registers. When the GCLR push-button switch is depressed, the message will stop scrolling. This CUPL design can be compiled using either the ProChip Designer or the Atmel-WinCUPL software.

The first section of the LOGIC_D8.PLD as shown below pre-defines which segments of the LED should be asserted in order to display the desired letter or number. For example, to display the upper case letter "C", segments A, D, E, and F need to be set to low (active low) and the remaining segments need to be set to high.

```
$define  Font0 'b'1000000  /* = (  _f_e_d_c_b_a );    0 */
$define  Font1 'b'1111001  /* = (        _c_b   );    1 */
            :
$define  FontA 'b'0001000  /* = (_g_f_e  _c_b_a );    A */
```

The next section of this CPLD design as shown below illustrates how to declare and assign pin numbers in the CUPL language to the input and output signals. The input and output pin assignments are assigned according to the connections between the CPLD and the eight 8-segment LED's as shown in the connection tables (Table 2-1 to Table 2-8) in Section 2.

```
/* Inputs */
pin  1  = GCLR; /* Global Clear input */
pin  83 = MCLK; /* Global Clock input */
pin  84 = GOE;  /* GOE1 button used as direction control */

/* Outputs */
/* DSP1 */
pin  49 = LED1A;       /* LED1 segment A */
pin  46 = LED1B;       /* LED1 segment B */
pin  48 = LED1C;       /* LED1 segment C */
pin  50 = LED1D;       /* LED1 segment D */
pin  52 = LED1E;       /* LED1 segment E */
pin  51 = LED1F;       /* LED1 segment F */
pin  54 = LED1G;       /* LED1 segment G */
```

Next, the buried signals for the counter and state machine are declared as PINNODE's as shown below. The feedback and/or the foldback paths available in each macrocell implement these buried signals. For the listing of the pinnode numbers, please refer to the "ATF15xx Device Help" section of the ProChip Designer Help File.

```
pinnode [618,634,650,687]= [CA20..CA17];
pinnode = [CA16..CA0];
pinnode = [SM7..SM0];
```

After assigning the input, output and buried signals, the related signals (i.e. the LED segments and buried counter) are grouped together as shown below to make the design source code more readable and manageable. In CUPL, the "Field" declaration can be used to group a specific set of signals.

```
Field DSP1  = [LED1G,LED1F,LED1E,LED1D,LED1C,LED1B,LED1A];
Field DSP2  = [LED2G,LED2F,LED2E,LED2D,LED2C,LED2B,LED2A];
      :
Field CNT_A = [CA20..CA0];
Field SM    = [SM7..SM0];
```

Next, a 21-bit buried up-counter implemented using D-type Flip-flops is shown below and it is used to divide the 2.0 MHz clock into a 0.954 Hz (2 MHz ÷ 2^{21} = 0.954 Hz) signal that can be used to display the text messages. The last bit of this counter is used as the clock for the state machine that controls the display sequence of the messages on the LEDs.

```
CA0.d = !CA0;
CA1.d = CA0 $ CA1;
      :
CA7.d = (CA6 & CA5 & CA4 & CA3 & CA2 & CA1 & CA0) $ CA7;
      :
CNT_A.ck = MCLK;
CNT_A.ar = !GCLR;
```

The next section of this PLD design is a state machine with 15 states to control the display sequence of the text messages on the LEDs. The GOE push-button switch on the CPLD Development/Programmer Board controls the flow of this state machine. When this switch is in the "up" position, the state machine will go from RESET to State-0 to State-1 to State-2 and so on until it reaches State-14 and then it will go back to State-0. On the other hand, if the GOE switch is in the "down" position, the state machine will go in the opposite direction (i.e. State-14 to State13 .. etc).

```
SM.ck = COUNTER_1;
sequence SM
{
      present RESET
                        next S0;
      present S0
           if  SM_DIR next S1;
           if !SM_DIR next S14;
           :
      present S14
           if  SM_DIR next S0;
           if !SM_DIR next S13;
}
```

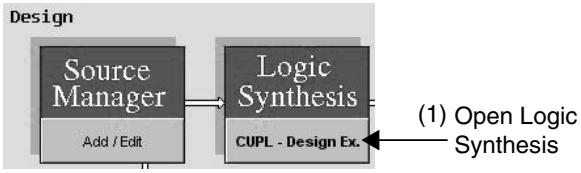
Finally, the last section of the PLD design will assign the appropriate letters or numbers to the eight 8-segment LEDs to be displayed during the different states of the state machine. The user can easily change the letters/numbers to be displayed by changing this section of the code to the appropriate pre-defined letters/numbers.

```
LED1 =    FontBK & SM:[RESET]
        # FontBK & SM:[S0]
        # FontLl & SM:[S1]
        # FontLo & SM:[S2]
        # FontLg & SM:[S3]
        # FontLi & SM:[S4]
        # FontLc & SM:[S5]
        # FontBK & SM:[S6]
        # FontLd & SM:[S7]
        # FontLo & SM:[S8]
        # FontLu & SM:[S9]
        # FontLb & SM:[S10]
        # FontLl & SM:[S11]
        # FontLi & SM:[S12]
        # FontLn & SM:[S13]
        # FontLg & SM:[S14];
```

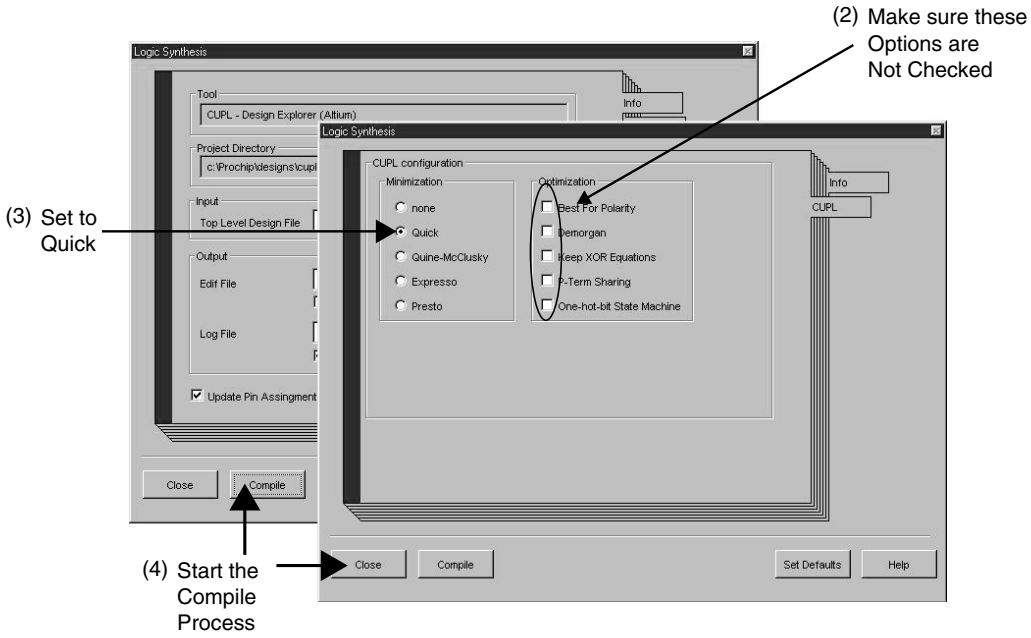
3.4 Compile the CUPL Design

In this part of the tutorial, the CUPL design will be compiled through the Logic Synthesis process into a set of optimized/minimized logic equations.

1. Click on the **CUPL – Design Ex**. button in the Design Flow Window to open the Logic Synthesis Window.



2. Make sure all of the options in the *Optimization* section are unchecked.
3. Make sure the *Minimization* setting is set to **Quick**.
4. Click on the **Compile** button to start the CUPL compile process.



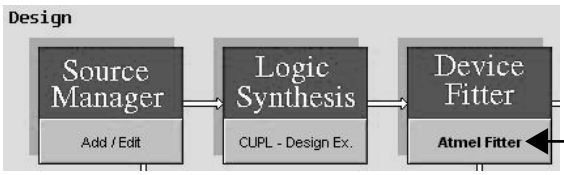
The user can click on the **Set Defaults** button and it will automatically specify the Synthesis tool in the Tool Text box.

If the user clicks on the CUPL Tab, it shows the various Synthesis options. Please refer to the HELP file for further description.

3.5 Fit the Synthesized Design File

In Section 3.4, the Logic Synthesis portion of the CPLD Design Flow was completed. On successful compilation, the CUPL compiler tool produces a PLA output file (with extension .pla). A PLA file contains the netlist of the optimized and minimized logic equations. It is now necessary to map this netlist into a specific Atmel PLD architecture using the **Atmel Fitter**.

1. The user can now proceed to the Device Fitter portion of the Design Flow by clicking on the **Atmel Fitter** button.

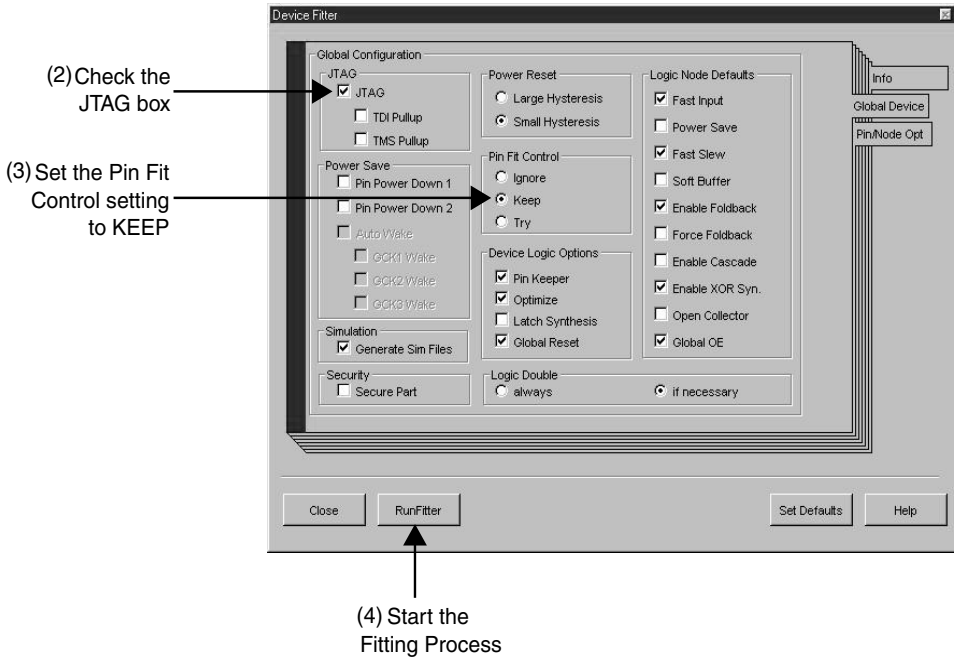


The user can either use the Default options or specify Fitter properties. ProChip Designer will automatically select the PLA file associated to the current design project and the tool type. In this example, since the target device is an ATF1508AS, the fit1508.exe device fitter will be selected.

The fitter creates the important JEDEC and FIT REPORT output files. They contain the data for programming the Device (using In-System Programming or on a third party device programmer) and the pin assignments required for board layout respectively.

Please review the Global Device Parameters and Pin/Node Options as well. The Help Files also show the Device Pin_Node lists for each of the ATMEL CPLDs.

2. Make sure the **JTAG** box is checked. This enables the JTAG port for ISP programming.
3. Make sure the *PIN FIT CONTROL* setting is set to **Keep**. This will ensure that the pin assignments in the PLD file will be kept during the Place-and-Route process.
4. When all the fitter options are set, click on the **Run Fitter** button to fit the design.



The Fitter Report (.FIT) File generated for this design is shown below.

```
Logic Array Block      Logic Cells    I/O Pins       Foldbacks      TotalPT        FanIN
 Cascades
A: LC1  - LC16          16/16(100%)    8/16(50%)      5/16(31%)      46/80(57%)     (19)    0
B: LC17 - LC32          16/16(100%)    8/16(50%)      3/16(18%)      51/80(63%)     (38)    0
C: LC33 - LC48          16/16(100%)    8/16(50%)      2/16(12%)      48/80(60%)     (38)    0
D: LC49 - LC64          16/16(100%)    6/16(37%)      2/16(12%)      40/80(50%)     (38)    0
E: LC65 - LC80          16/16(100%)    6/16(37%)      6/16(37%)      55/80(68%)     (32)    0
F: LC81 - LC96          16/16(100%)    8/16(50%)      2/16(12%)      47/80(58%)     (38)    0
G: LC97 - LC112         16/16(100%)    8/16(50%)      3/16(18%)      43/80(53%)     (25)    0
H: LC113- LC128        16/16(100%)    8/16(50%)      2/16(12%)      42/80(52%)     (34)    0


Total dedicated input used:   3/4     (75%)
Total I/O pins used           60/64   (93%)
Total Logic cells used        128/128 (100%)
Total Flip-Flop used          31/128  (24%)
Total Foldback logic used     25/128  (19%)
Total Nodes+FB/MCells         153/128 (119%)
Total cascade used            0
Total input pins              7
Total output pins             56
Total Pts                     372
 :
```

The ATF15xx Family devices Logic Doubling features provide extra I/O connectivity and logic reusability. Some of the Logic Doubling features available in the ATF15xx family of CPLDs are:

- Bury either Register or Combinatorial signal while using the other for output
- Dual independent feedback allows multiple latch functions per macrocell
- 5 product terms per macrocell, expandable to 40 per macrocell with cascade logic, plus 15 more with foldback logic
- D/T/Latch configurable flip-flops plus transparent latches
- Global and/or per macrocell Output Enable
- Single level Switch Matrix
- Up to 40 inputs per Logic Block

In the LOGIC_D8.PLD example given in this tutorial, Logic Blocks B, C D, and F have 37 or more signal inputs (Fan-In's) as shown in the Universal-Interconnect-Multiplexer assignments section of the .FIT file. The availability of wide Fan-In's to the Logic Blocks is one of the many Logic Doubling features. This feature improves the possibility of routing all the necessary signals from the Global Bus to the Logic Blocks.

In addition, macrocells 37 and 59 of the ATF1508 are able to implement both combinatorial outputs (LED1G and LED8D) and buried registered signals (CA0 and RST) within the same macrocells. This is shown in the Resource Usage section of the .FIT file.

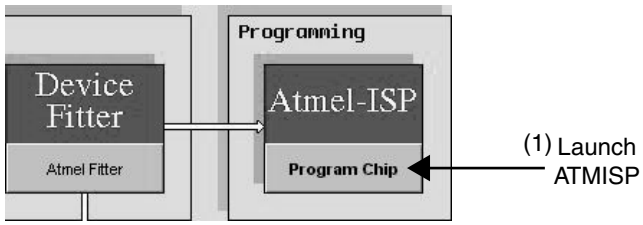
For more examples of design techniques that utilize the Logic Doubling features of the ATF15xx Family, refer to Atmel's Logic Doubling White Paper and Reference Designs available on the Atmel website. These examples show how to apply Logic Doubling techniques to new product designs, to obtain the benefits of more features in a smaller and possibly less expensive chip, or spare logic resources for future revisions and reduce the risk of PCB re-spin.

3.6 Program and Verify Design

In this step of the tutorial, the user will program an ATF1508AS 84-pin PLCC device on the Atmel CPLD Development/Programmer Board through ISP and then verify the design by observing the text messages displayed on the eight 8-segment LED displays of the CPLD Development/Programmer Board.

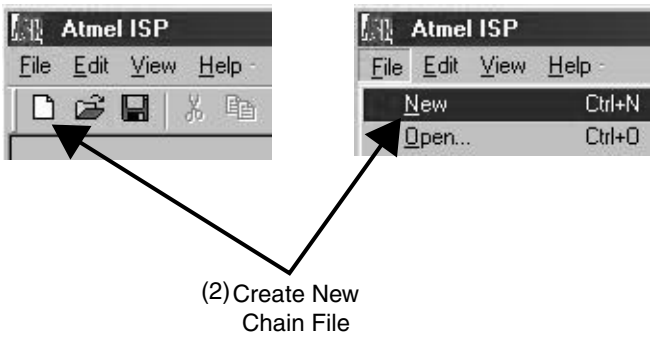
The user will need to follow the steps below to setup the ATMISP software in order to program the ATF1508AS 84-pin PLCC on the CPLD Development/Programmer Board.

1. To create a new chain file, the **ATMISP Software** first needs to be launched either through the **PROGRAM CHIP** button in the ProChip Designer window, the ATMISP desktop icon or the *Start ... Programs .. Atmel ISP* menu.

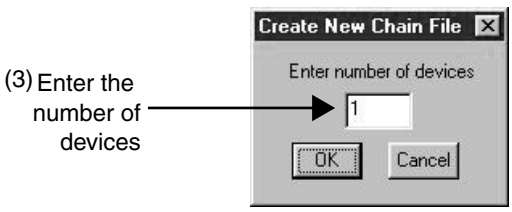


If ATMISP is launched through ProChip Designer, steps 2 to 6 below can be skipped since ProChip Designer will automatically setup the appropriate chain file for the ISP operation.

2. To create a new chain file, select the **New** command under the **File** menu or click on the **New Shortcut Button**.

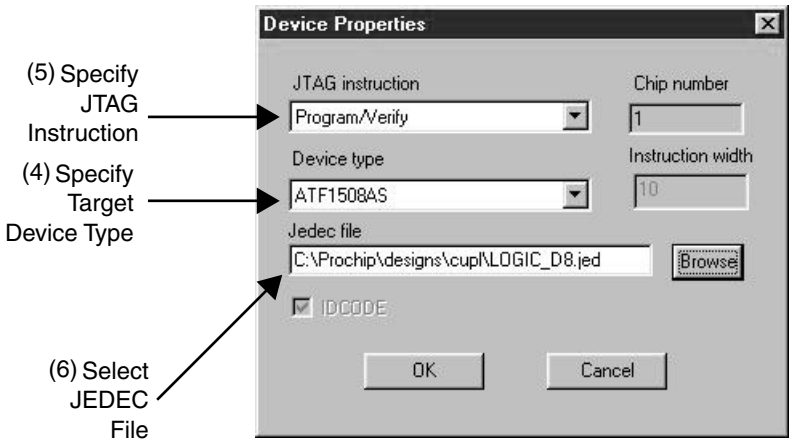


3. The first piece of information that the software asks for when creating a new chain is the number of devices in the JTAG chain. Therefore, enter **1** and then click **OK** since a 1-device JTAG chain will be programmed.



4. Next the user will need to specify the properties of each JTAG device in the Device Properties window. First, select the target device type of the first device in the JTAG chain. For this tutorial, please select **ATF1508AS** as the target device type.
5. In the JTAG Instruction field, the user can specify the appropriate JTAG instruction to be executed on this device in the chain. Please select **Program/Verify** to program and verify the ATF1508AS.

6. The next step is to specify the JEDEC file to be programmed into the target device in the JEDEC File field. Click on the Browse button, change the directory to **[..\PROCHIP\DESIGNS\CUPL"]** and then select **LOGIC_D8.JED** as the target JEDEC file. Click **OK** to close the JTAG Device Properties window when all properties are specified.



The next few steps require the user to setup the Atmel CPLD Development/Programmer Board to program the ATF1508AS through ISP.

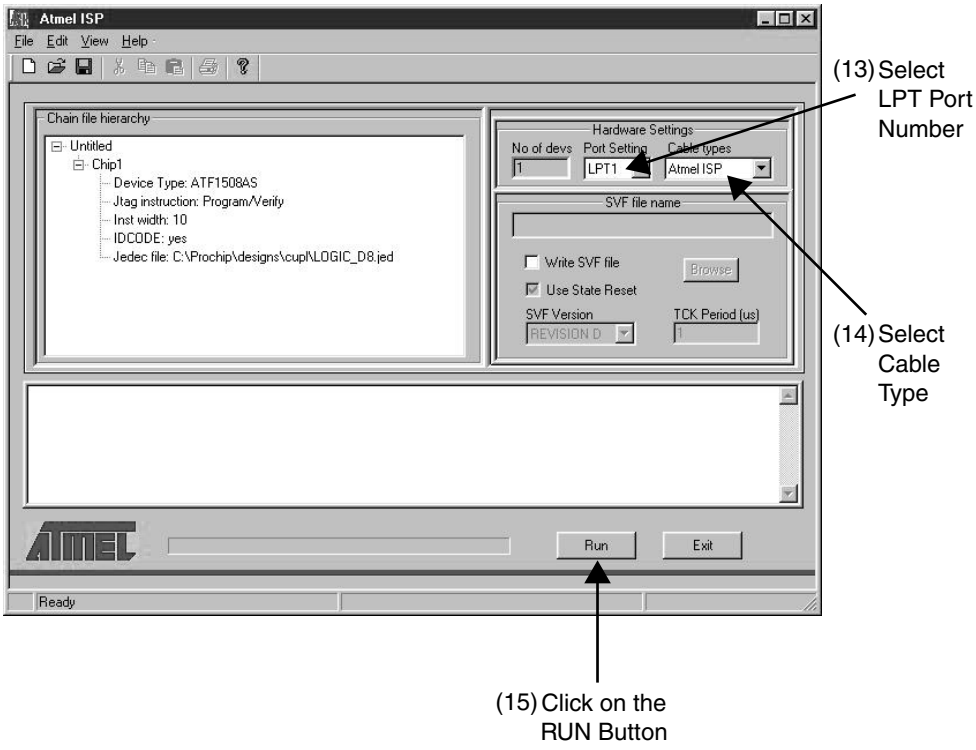
7. Connect the 25-DB side of the Atmel-ISP Cable to the PC's parallel port and the 10-pin header side of the Atmel-ISP Cable to the Atmel CPLD Development Board as shown Figure 2-5.
8. Connect a **9V** AC/DC power adapter to the power connector (JPower) of the Atmel CPLD Development/Programmer Board.
9. Set the 5V/3.3V jumper to **5V**. This will set the system board V_{CC} to 5V.
10. Set the JPCLK jumper to **GCLK1** so that the output of the crystal oscillator will be connected to Pin 83 of the ATF1508AS.
11. Connect the 84-pin PLCC Socket Adapter Board onto the main Development/Programmer Board.

Note: If a device in a different package type is to be programmed, then the appropriate Socket Adapter Board must be used.

12. Switch the Power Switch to the **ON** position.
13. Select the appropriate LPT port in the *Port Setting* field. **LPT 1** is the default port.
14. Select the **ISP** download cable type in the *Cable Types* field. The default cable type is the Atmel ISP Cable but it can be changed to the Altera ByteBlaster cable if the ByteBlaster cable is being used.

Now both the user's software and hardware are setup for ISP programming, and the user can execute the **PROGRAM/VERIFY** instruction to program the ATF1508AS on the Atmel CPLD Development/Programmer Board.

15. Click on the **Run** button in the ATMISP main window to execute the JTAG instruction to program the ATF1508AS on the CPLD Development/Programmer Board.



After successfully programming the ATF1508AS with the LOGIC_D8.JED file, the eight 8-segment LED's will display the words "Logic Doubling".

If these two text messages are correctly displayed on the CPLD Development/Programmer Board, then the user has successfully completed this tutorial.

Section 4

Schematic Diagrams

Figure 4-1. Schematic Diagram of the Atmel CPLD Development/Programmer Board

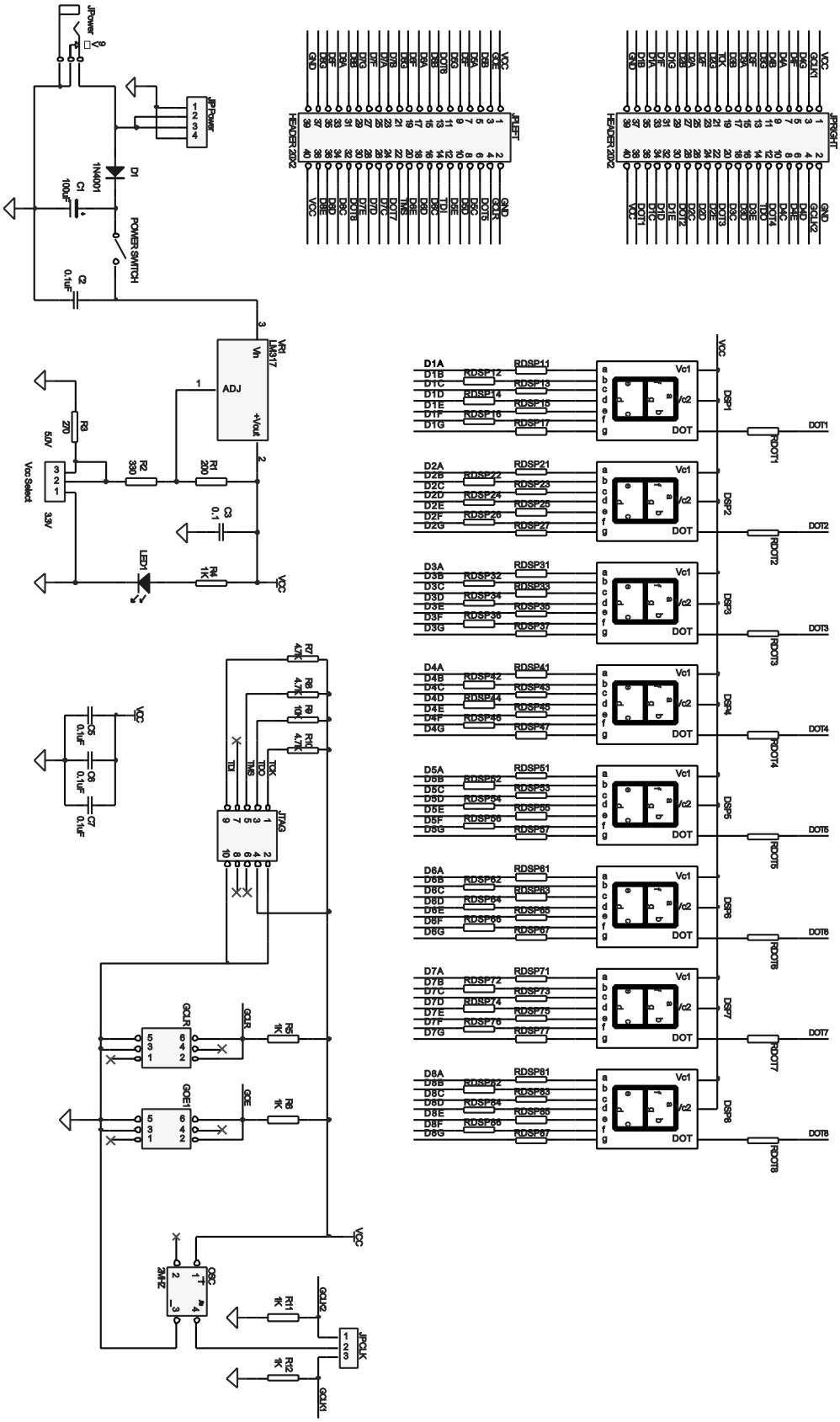


Figure 4-2. Schematic Diagram of 44-pin PLCC Socket Adapter Board

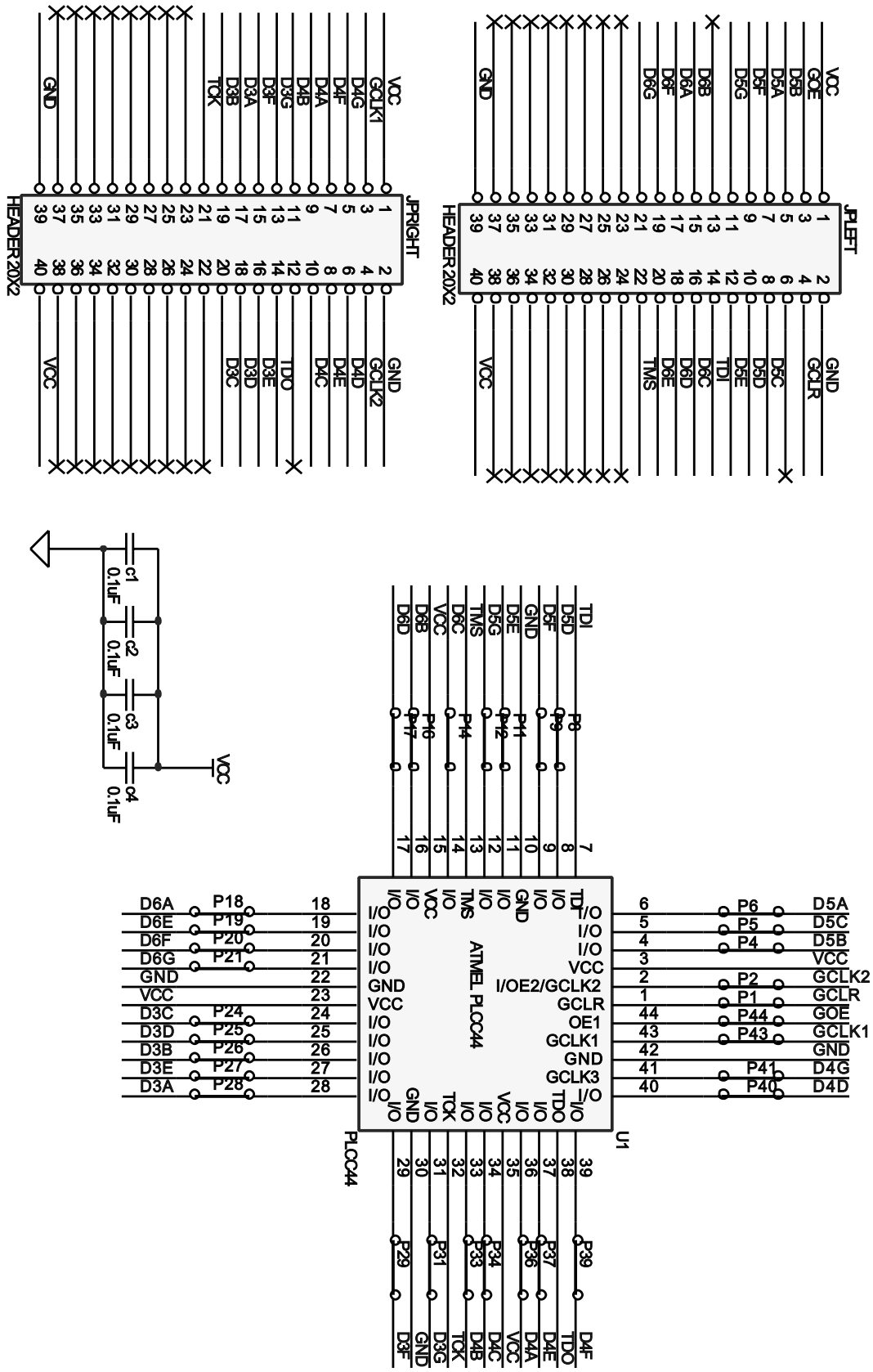


Figure 4-3. Schematic Diagram of 44-pin TQFP Socket Adapter Board

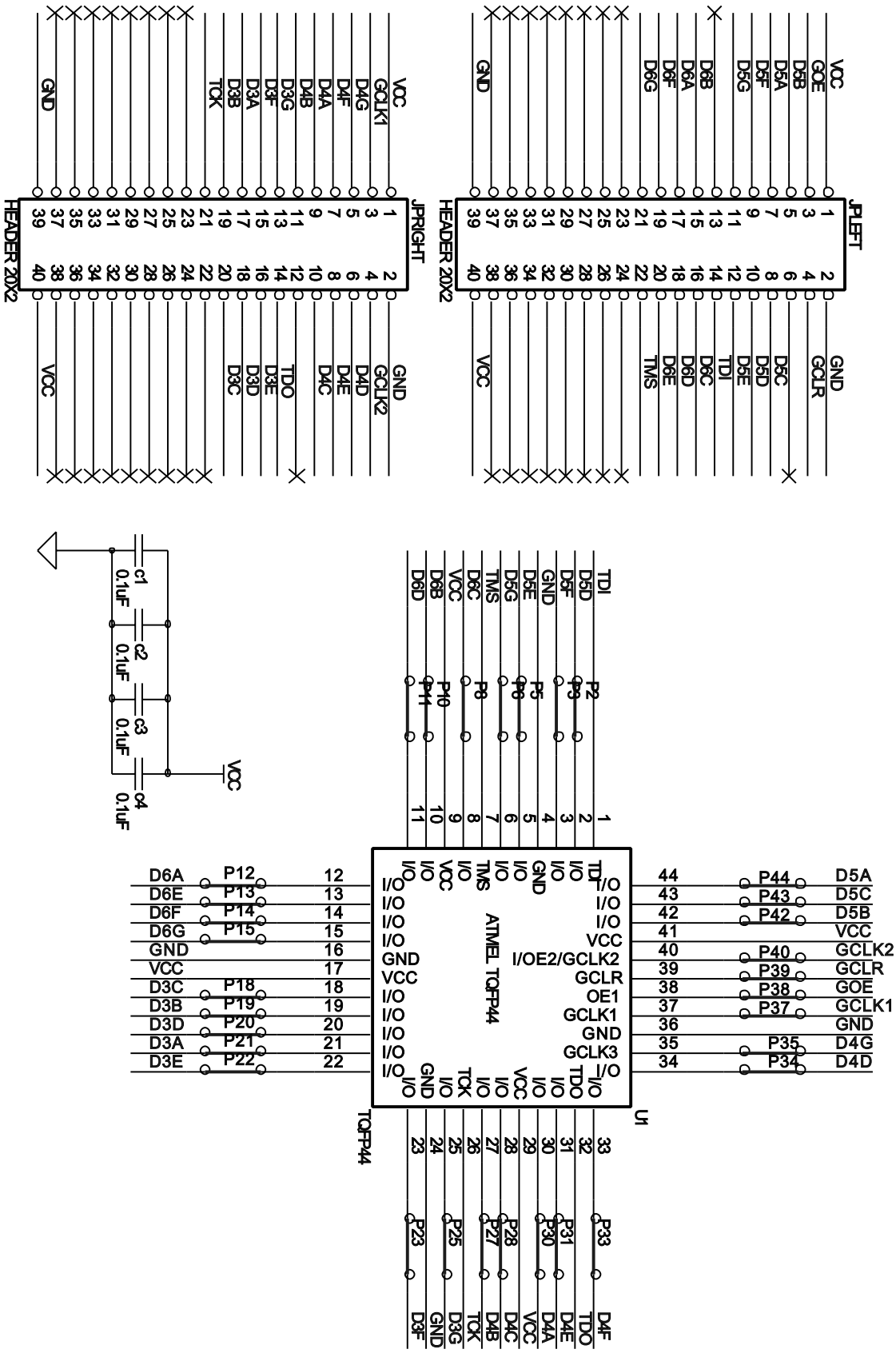


Figure 4-4. Schematic Diagram of 68-pin PLCC Socket Adapter Board

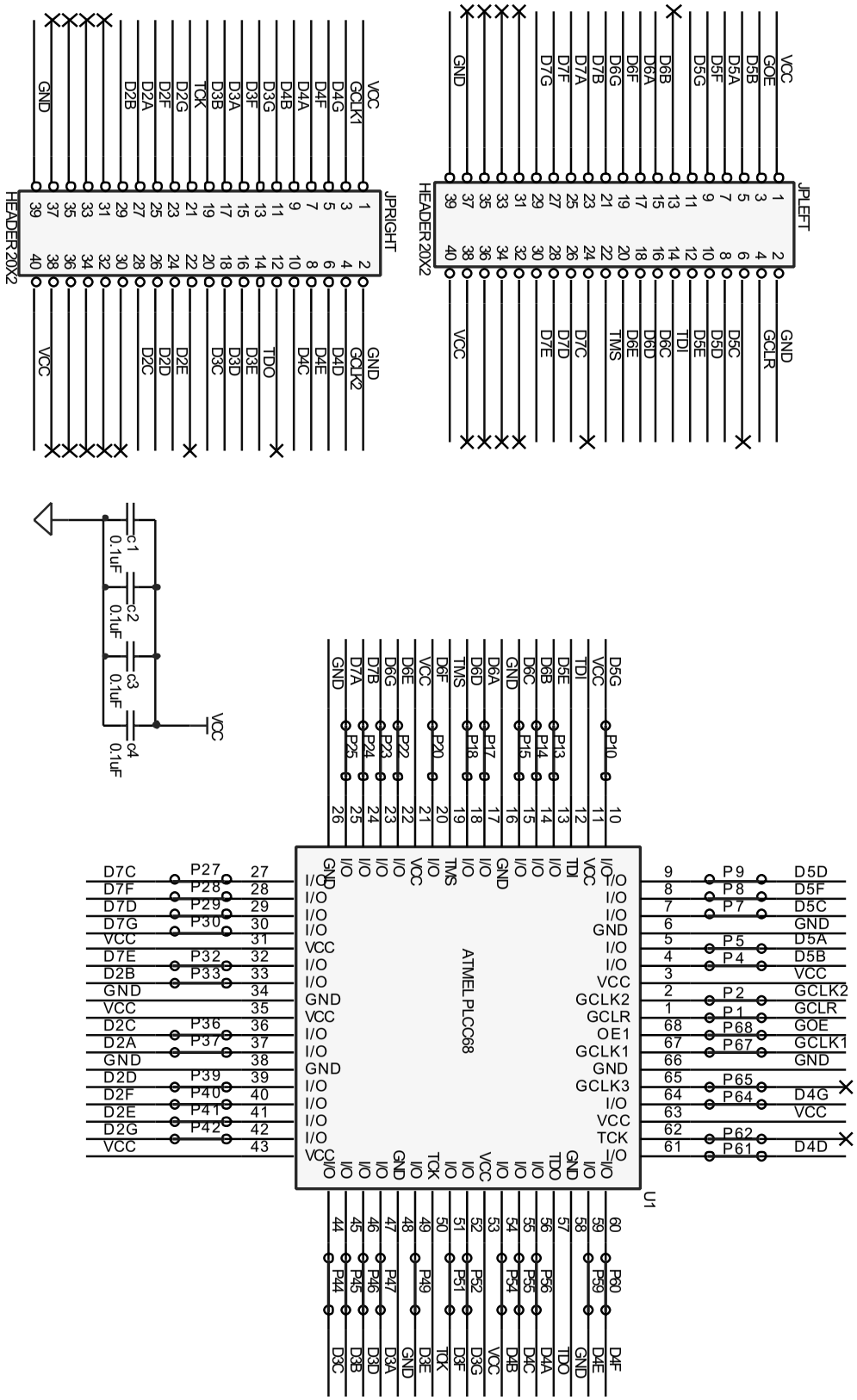


Figure 4-5. Schematic Diagram of 84-pin PLCC Socket Adapter Board

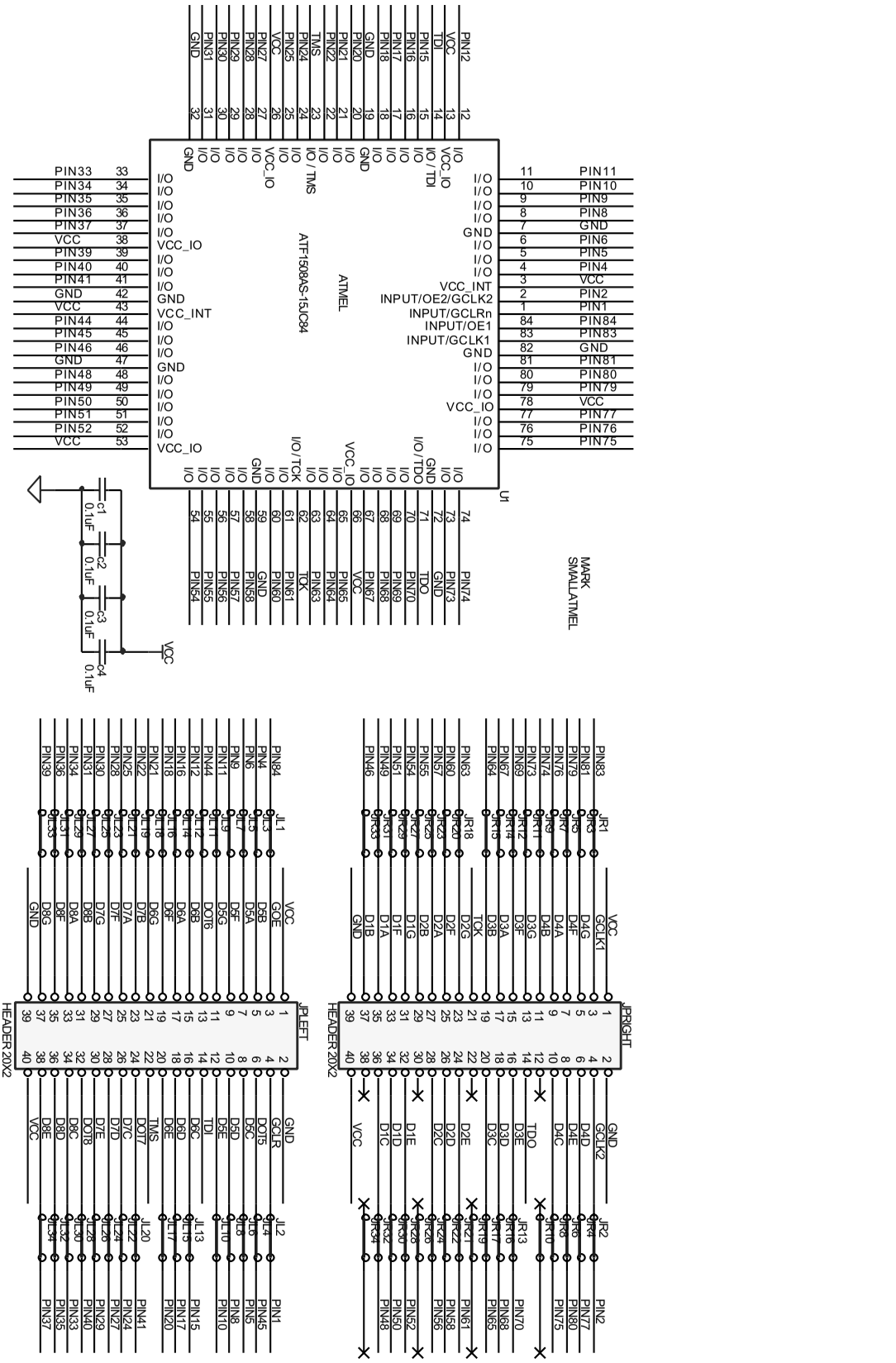


Figure 4-6. Schematic Diagram of 100-pin PQFP Socket Adapter Board

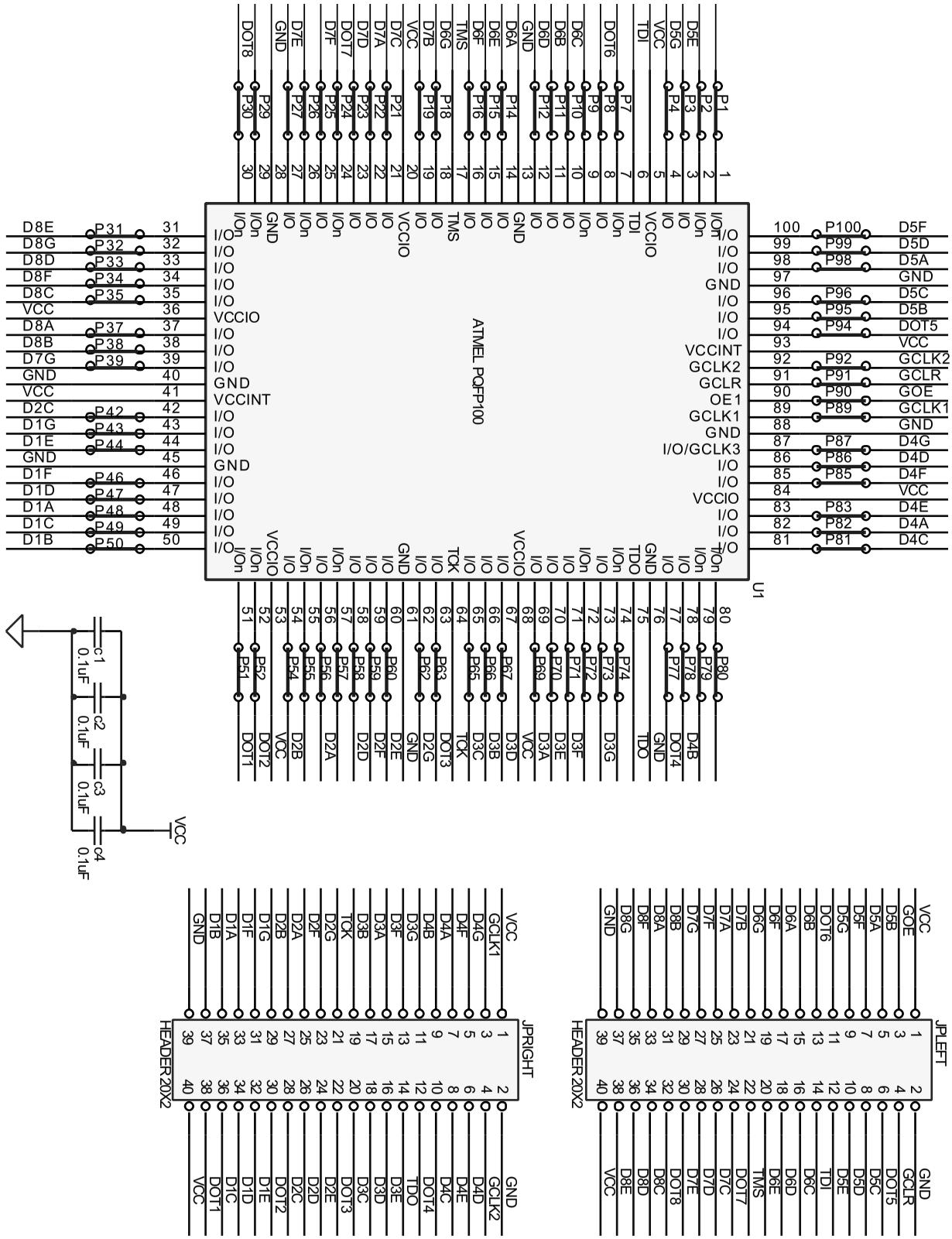


Figure 4-7. Schematic Diagram of 100-pin TQFP Socket Adapter Board

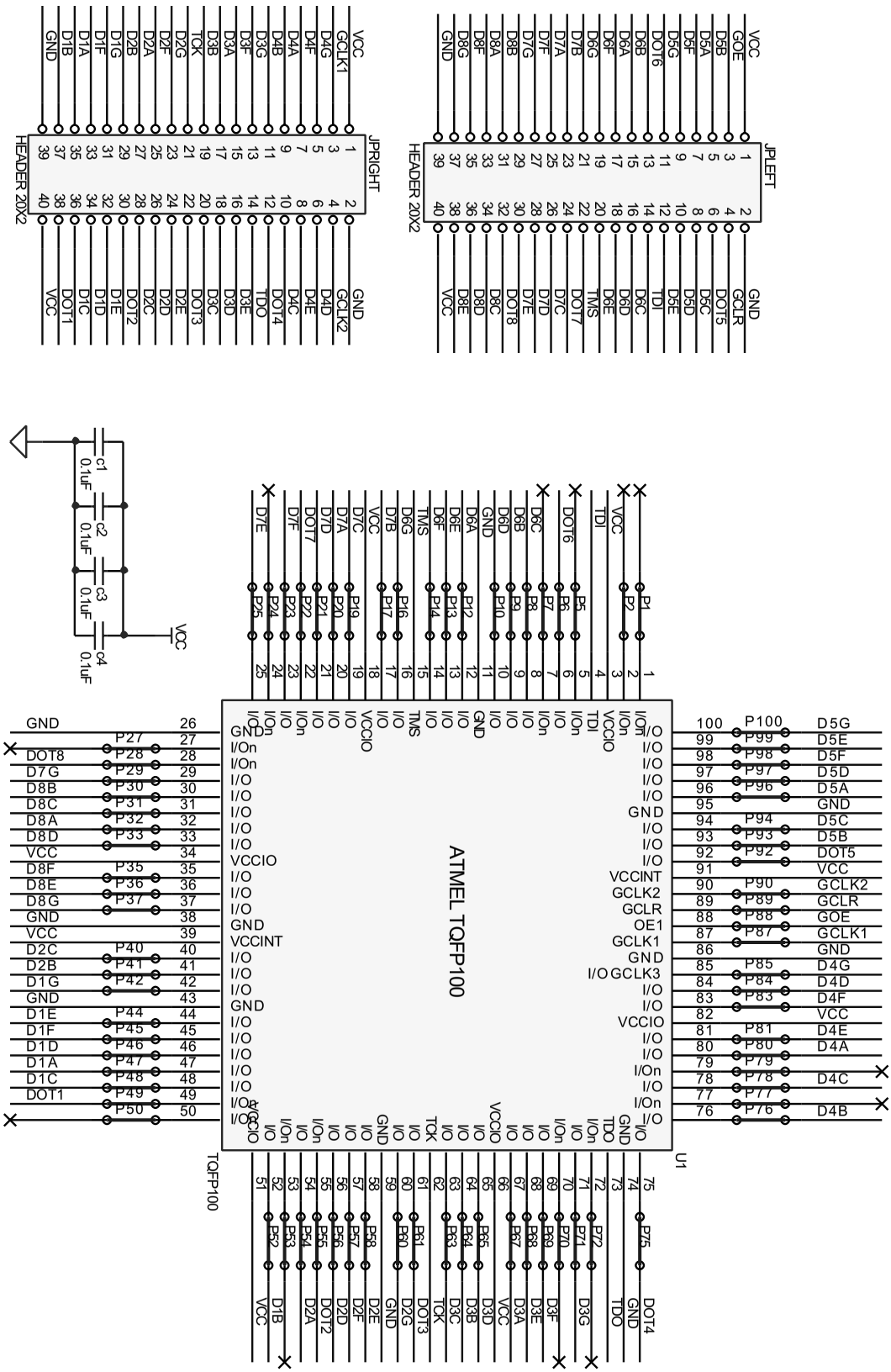


Figure 4-8. Schematic Diagram of 144-pin TQFP Socket Adapter Board

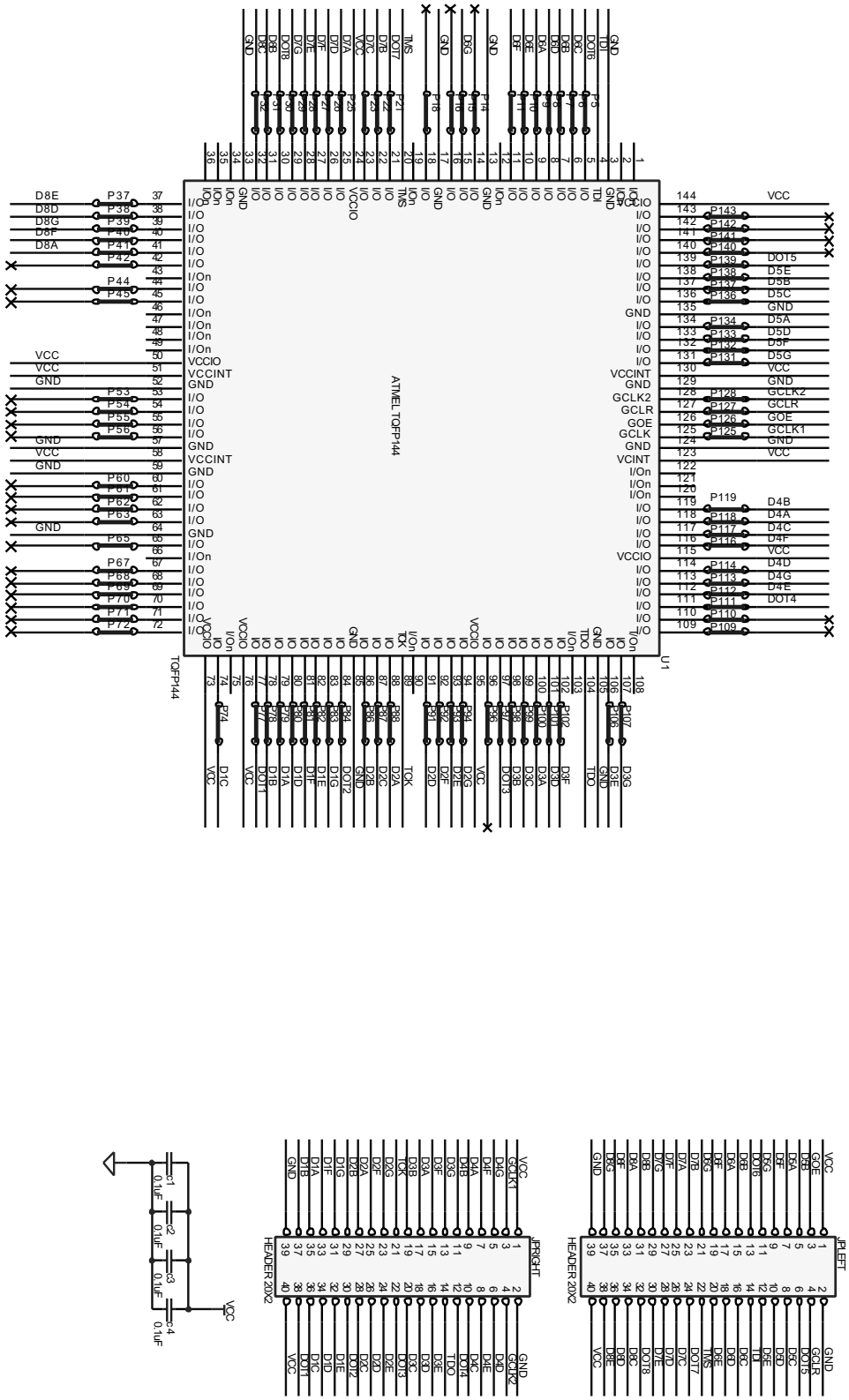


Figure 4-9. Schematic Diagram of 160-pin PQFP Socket Adapter Board

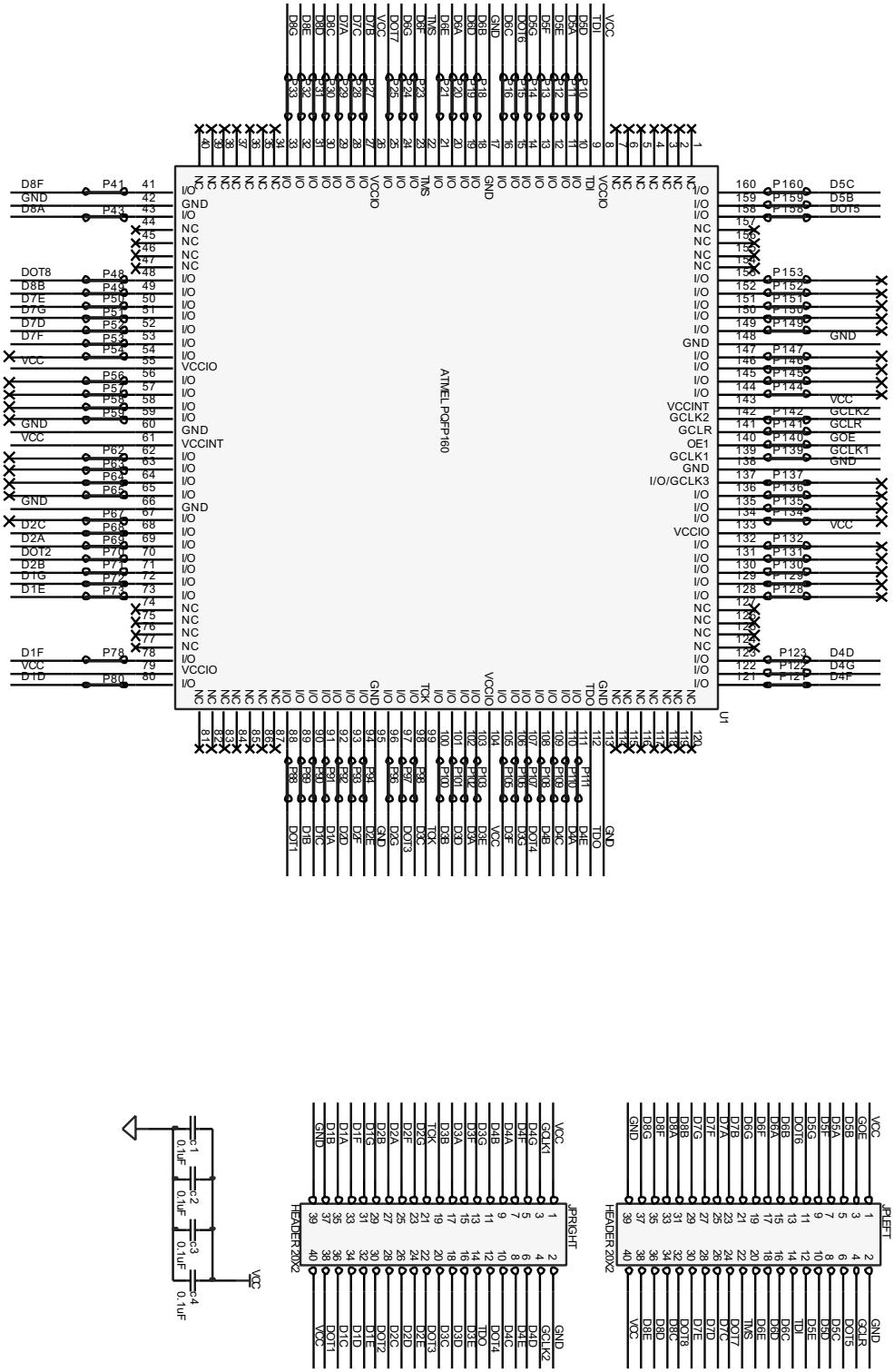


Figure 4-10. Schematic Diagram of Atmel CPLD ISP Cable

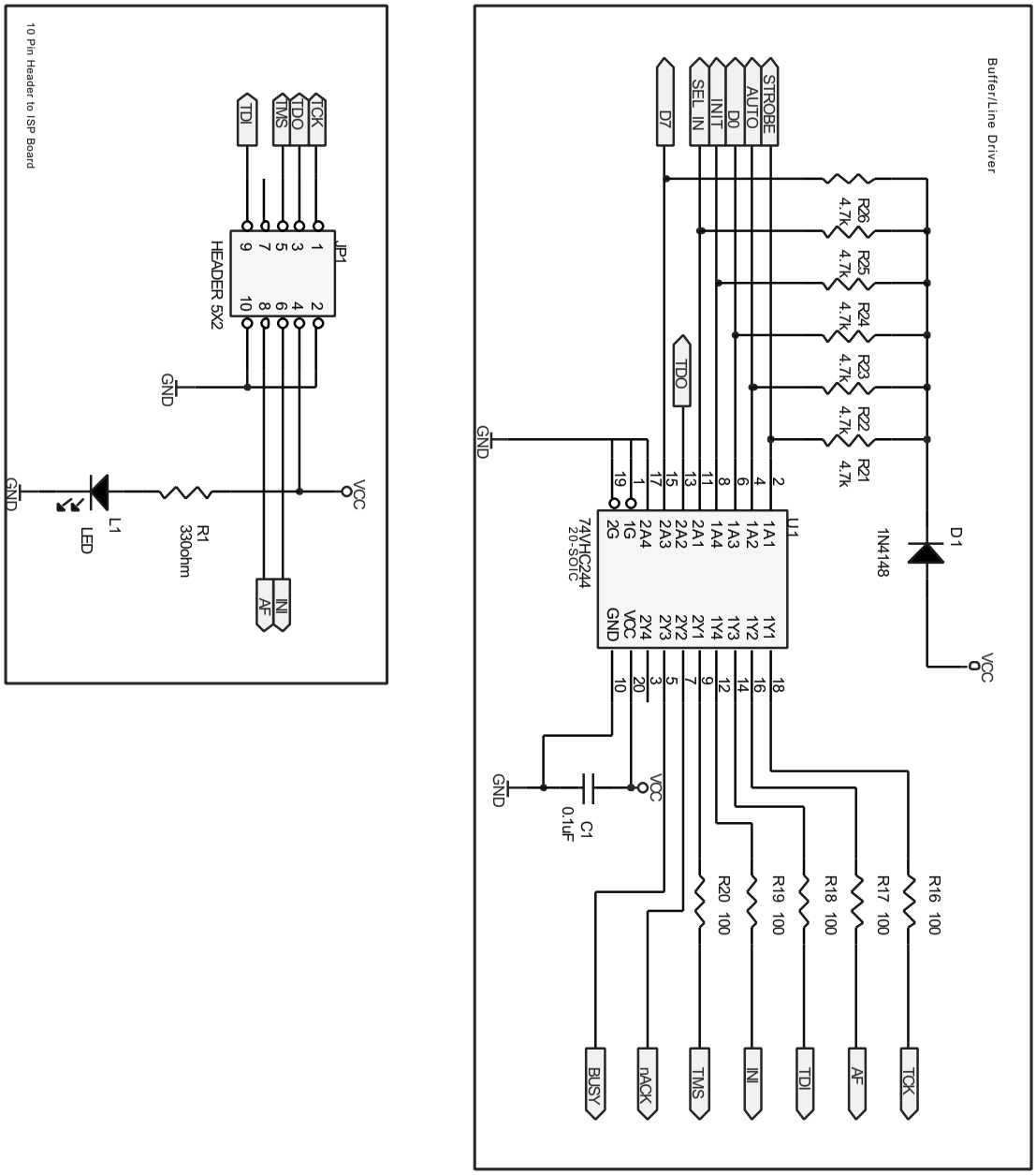
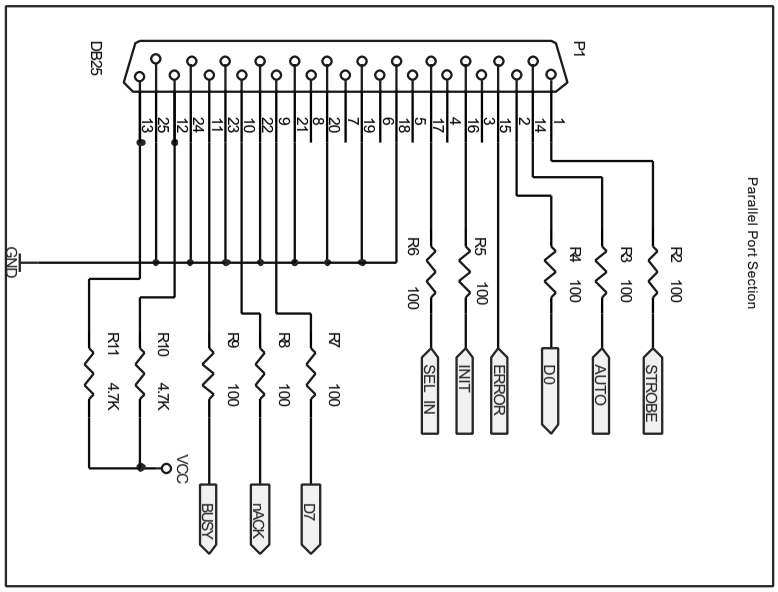
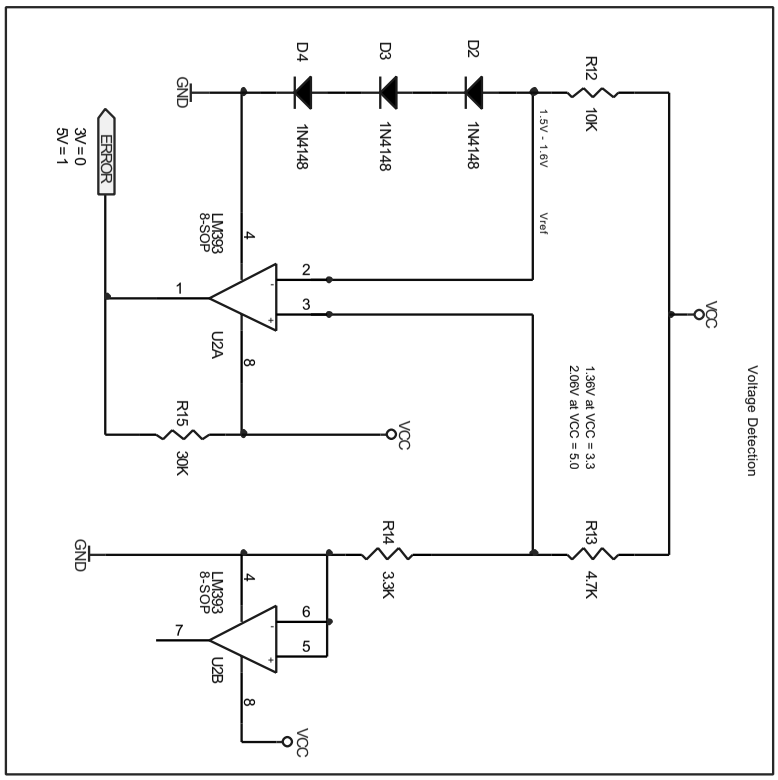


Figure 4-11. Schematic Diagram of Atmel CPLD ISP Cable, Continued





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